# **DEPARTMENT OF THE ARMY TECHNICAL MANUAL**

# **FIELD AND DEPOT MAINTENANCE**

# **RADAR TEST SET**

# **AN/UPM-60A**

*HEADQUARTERS, DEPARTMENT OF THE ARMY NOVEMBER 1959*

## **WARNING**

# **DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT**

**Be careful when working on the -300-volt and -450-volt plate and power supply circuits, or on the 115-volt ac line connections. Serious injury or death may result from contact with these voltages.**

# **DON'T TAKE CHANCES!**



**TM6625-228-35-1**



<span id="page-2-0"></span>*Figure 1. Radar Test AN/UPM-60A, block diagram.*

# TECHNICAL MANUAL  $\Big]$ DEPARTMENT OF THE ARMY No. 11-6625-228-35 WASHINGTON 25, D.C., *17 November 1959*

# <span id="page-3-0"></span>**RADAR TEST SET AN/UPM-60A**

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#### <span id="page-4-0"></span>**THEORY**

#### <span id="page-4-1"></span>**Section I. BLOCK DIAGRAM**

#### <span id="page-4-2"></span>**1. Scope**

- *a. Manual.*
	- (1) This manual covers field and depot maintenance for Radar Test Set AN/UPM-60A. It includes instructions appropriate to third, fourth, and fifth echelons for troubleshooting, testing, alining, and repairing the equipment, replacing maintenance parts, and repairing specified maintenance parts. It also lists test equipment for third, fourth, and fifth echelon maintenance. Detailed functions of the equipment are covered in the theory section.
	- (2) The complete technical manual for this equipment includes two other publications

TM 11-6625-228-12. TM 11-6625-228-12P.

(3) Forward comments concerning this manual to the Commanding Officer, U. S. Army Signal Publications Agency, Fort Monmouth, N. J.

*Note.* **For applicable forms and records, see paragraph 2, TM 11-6625-228-12.**

- <span id="page-4-3"></span>*b. Theory.*
	- (1) *Signal paths in power-meter operation* [\(fig. 1\).](#page-2-0)
		- (*a*) When the test set is used to measure the output power of a radar transmitter, input signals are coupled to the input-output waveguide section through the RF connector and through a calibrated variable attenuator (AT2) to a temperature compensated power monitor. The power monitor consists of a bridge circuit and a power-level indicating meter calibrated in milliwatts and dbm (decibels relative to 1 milliwatt).
		- (*b*) The radio frequency (RF) shutter prevents the output Dower of the radar transmitter from reaching the

klystron oscillator. The frequency meter (Z2) is detuned to insure an accurate power reading.

- (2) *Signal paths in frequency-meter operation* [\(fig. 1\)](#page-2-0).
	- *(a)* When the test set is used as a frequency meter, an absorption type frequency meter is tuned to resonance. The resonant frequency meter cavity causes a reduction of power level in the microwave section. This reduction of power at the resonant frequency shows up as a dip on the power meter (power monitor bridge). The resonant frequency (in megacycles) is indicated directly on a front panel counter which is geared to the tuning mechanism of the cavity.
	- *(b)* When measuring the frequency of a radar transmitter, the signal path is the same as described in (1) (*a*) above. When a sharp deflection occurs on the power meter, the frequency meter is tuned to the transmitter frequency. The frequency of the transmitter can be determined by reading the frequency on the WAVEMETER FREQUENCY dial.
	- *(c)* When measuring an external signal of unknown frequency, the signal path and method are the same as described in (*b*) above.
	- *(d)* When measuring the frequency of the klystron oscillator, the output signals from the klystron oscillator pass through the power set attenuator (AT3) to the RF shutter; this allows the klystron signals to reach the frequency meter (Z2), the power monitor bridge, and the RF connector. The frequency of the

klystron oscillator is measured when the frequency meter (Z2) causes a sharp deflection on the power meter.

- (3) *Signal paths in signal-generator operation* [\(fig. 1\)](#page-2-0).
	- (*a*) When the test set is used to measure the frequency of a radar receiver, synchronizing signals from the radar set are coupled to the INPUT SYNC jack, and thus produce delayed and undelayed triggers at jacks J10 and J11 respectively. The undelayed trigger is used to synchronize an oscilloscope with the test set and radar set. The delayed trigger produces sawtooth signals which modulate the klystron oscilator. Synchronized FM microwave signals from the klystron oscillator are attenuated by the POWER SET attenuator (AT3) to a 1-milliwatt reference level, and are allowed by the RF shutter to reach the frequency meter, power monitor bridge, and the RF connector. The microwave signals of known frequency and power are coupled from the RF connector to the radar receiver, producing false echoes which will appear as a target on the oscilloscope. When the wavemeter (Z2) is tuned to the frequency of the microwave signal, a dip will appear on the peak of the false target The WAVEMETER FREQUENCY dial will indicate the frequency to which the radar receiver is tuned.
	- (*b*) To measure the frequency bandwidth of a radar receiver, the signal generator is tuned to the radar receiver frequency, producing a false target as described in *(a)* above. The wavemeter is detuned and the peak of the false target is marked on the oscilloscope screen. The output of the signal generator is reduced to .5 milliwatts (-3 dbm) and the peak of the false target is marked on the oscilloscope screen. The second marking represents the half-power points. The output of the signal generator is increased to 1

milliwattt. The bandwidth of the radar receiver can be determined by noting on the WAVEMETER FREQUENCY dial when the frequency dip falls at the two halfpower points near the ends of the band-pass curve (false target). The difference between the readings obtained at the two points is the frequency bandwidth of the radar receiver.

(*c)* To measure the sensitivity of a radar receiver, the signal generator is tuned to the radar receiver frequency, producing a false target as described in (*a*) above. The output power of the signal generator is set at 1 milliwatt (0 dbm). When the grass (noise) level of the radar receiver has been set correctly, the ATTENUATOR control is increased (signal generator power decreases) until the false target just disappears into the grass level. The receiver sensitivity figure is obtained by adding the POWER DBM dial reading, attenuation losses introduced in coupling the signal to the receiver, and the dbm correction figure of the test set. The total figure is the minimum power level in dbm below 1-milliwatt at the receiver input necessary to produce a minimum discernable signal indication.

# <span id="page-5-0"></span>**2. Block Diagram Discussion**

[\(fig. 1\)](#page-2-0)

The radar test set is a power meter, frequency meter, and microwave signal generator used to test the performance of radar transmitters and receivers. Signal paths and wave forms are shown the block diagram [\(fig. 1\)](#page-2-0) and are described in *a* through *aa* below. The timing of the waveforms developed is illustrated i[n figure 2](#page-9-1) and discussed in [paragraph 3.](#page-8-1) For more detailed circuit information, refer to [paragraphs 4](#page-9-0) through [27](#page-31-0) and to figure 62.

<span id="page-5-1"></span>*a. Crystal Detector*. Crystal detector CR1 is mounted in a section of waveguide that is iriscoupled to the input-output waveguide. A type 1N26 silicon rectifier crystal detects RF power fed into the RF connector on the front panel. The resultant positive video output from the crystal is fed to the pulse amplifiers.

*b. Pulse Amplifiers.* Two pulse amplifier stages (V2 and V3) use high-transconductance type 6AH6 tubes as preamplifiers for the detected RF pulses received from the crystal detector. A positive video pulse output from V3 is fed to sync amplifier V101A. The pulse amplifiers operate only when the SYNC SELECTOR switch is in the EXT RF position. Cathode voltage (-300 volts) is removed in any other position of the switch.

*c. Sync Amplifier V101A.* The sync amplifier accepts either the positive output of the pulse amplifiers, or an external positive or negative synchronizing pule or sine wave from INPUT SYNC jack J6. The signals are amplified and applied to the trigger generator consisting of V101B and V102A. When the input to the sync amplifier is either an external *negative* synchronizing pulse or a sine wave, the resultant positive pulse or sine wave output is fed through contact 2 of SYNC SELECTOR switch S102B (Y segment) to V101B (the section of the trigger generator that is normally cut off) to initiate multivibrator action. When the input to the sync amplifier is either an external *positive* sychronizing pulse or the *positive* pulse output of the pulse amplifiers, the resultant *negative* pulse output is fed through contacts 1 or 3 of SYNC SELECTOR switch S102B (Y segment) to V102A (the section of the trigger generator that is normally conducting) to initiate multivibrator action.

*d. Rate Multivibrator V107*. Rate multivibrator V107 uses a dual-triode type 12AT7WA electron tube as a free-running pulse generator. Tube V107 develops the internal initiating pulse for application to the trigger generator when the SYNC SELECTOR switch is in either the INT X 1 or the INT X 10 position. The pulse repetition rate is adjustable between 100 and 10,000 pulses per second (pps) by the RATE control in conjunction with SYNC SELECTOR switch S102. A negative pulse is taken from V107B and fed through contacts 4 or 5 of S102A (X segment) to V102A (the section of the trigger generator that is normally conducting).

*e. Trigger Generator V101B and V102A.* The trigger generator circuit uses one section each of two dual-triode type 12AT7WA electron tubes in a pulse-shaping circuit. The trigger generator is triggered by the output of either the sync amplifier or the rate

multivibrator. The repetition rate of the resultant constantamplitude pulse output of the trigger generator is thus synchronized with either an external RF pulse, video pulse, sine wave, or the internal rate multivibrator output. The pulse output is differentiated and the negative peak clipped. The positive peak of the trigger generator output coincides in tine with the leading edge of the input trigger and is applied to V103A for amplification.

*f. Trigger Amplifier V103A*. Trigger amplifier V103A amplifies the positive peak of the differentiated wave from trigger generator V102A. The negative output pulse from trigger amplifier V103A is inverted by transformer coupling and applied as a positive pulse to the grid of undelayed sync generator V103B. Tube V103A is cut off when MODULATION SELECTOR switch S103 is in the CW position.

*g. Undelayed Sync Generator V103B*. The undelayed sync generator is a triggered blocking oscillator circuit and is driven by positive pulses from trigger amplifier V103A. The resultant positive output from the cathode of V103B has a pulse repetition rate that is identical with that of the signal input to the trigger generator and coincident in time with the leading edge of the input signal. The positive output pulses from the cathode of V103B are fed to UNDELAYED OUTPUT SYNC jack J11 and the delay phantastron circuit.

*h. Cathode Follower V104A*. This stage is used as a speed-up cathode follower for minimizing the delay generator recovery time.

*i. Delay Phantastron V105.* The positive output pulse from undelayed sync generator V103B triggers the monostable cathode-coupled phantastron circuit. The repetition rate of the output pulses of the delay phantastron is identical with the repetition rate of the trigger generator driving pulses. The output of the delay phantastron is a positive pulse whose leading edge coincides with the input trigger and whose width is variable. The width of the positive output pulse is determined by the setting of the DELAY MULTIPLIER switch and is varied by the DELAY control. The delay phantastron output at the screen grid is fed through trigger amplifier V104B to delayed sync generator V106A.

*j. Trigger Amplifier V104B*. Trigger amplifier V104B amplifies the negative peak of the differentiated wave from delay phantastron V105. The delayed positive trigger is fed to delayed sync generator V106A.

*k. Delayed Sync Generator V106A*. Delayed sync generator V106A is a triggered blocking oscillator circuit. The positive output trigger of trigger amplifier V104B is coupled to the grid of delayed sync generator V106A. The positive pip at the grid of V106A, which coincide in time with the variable trailing edge of the delay phantastron output, triggers V106A. Two outputs are obtained from V106A: A sharp positive pulse is obtained from the cathode, and a negative exponential wave is obtained from the grid. Both outputs have a repetition rate identical with the delay phantastron output and a delay time determined by the delay phantastron output. The positive pulse output of the delayed sync generator is fed to DELAYED OUTPUT SYNC jack J10 and to keyer trigger generator V109. The negative exponential output is fed to trigger amplifier V106B.

*l. Trigger Amplifier V106B*. Trigger amplifier V106B amplifies the negative exponential signal from the delayed sync generator. The positive pulse is fed to the frequency modulated (FM) generator V108B.

*m. FM Generator V108B*. FM generator V108B is a sawtooth generator. The positive pulse from delayed trigger amplifier V106B causes the stage to operate. Synchronization between the delayed trigger pulse repetition rate and the FM sweep rate (100 to 10,000 sweeps per second) is controlled by the RATE control and the MODULATION SELECTOR switch in the FM X 1 and FM X 10 positions. The amplitude of the sawtooth output from the FM generator is controlled by the FM AMPLITUDE control. This controlled sawtooth is then fed to FM amplifier V108A.

*n. FM Amplifier V108A*. FM amplifier V108A amplifies the sawtooth output of the FM generator. When the MODULATION SELECTOR switch is placed in position FM X 1 or FM X 10, the controlled output of the FM amplifier is applied to the reflector plate of klystron oscillator V1; it determines the amnlitude of the sawtooth voltage and the frequency deviation of the klystron oscillator.

*o. Keyer Trigger Generator V109*. Keyer trigger generator V109 is another triggered blocking oscillator circuit. The pulse repetition rate is controlled by the sharp positive pulses received from the delayed sync generator. The negative pulsed output of the keyer trigger generator is fed to the width multivibrator consisting of V110 and V111.

*p. Width Multivibrator V110 and V111*. The width multivibrator uses two pentodes in a monostable multivibrator circuit. The repetition rate is controlled by the repetition rate of the negative driving pulses from the keyer trigger generator. The width of the negative multivibrator output pulse is adjustable between .2 and 2 microseconds by the PULSE WIDTH control. The negative pulse is then fed to keyer V112.

*q. Keyer V112*. The keyer stage is a cathode follower circuit used to apply the negative pulse from the width multivibrator to klystron oscillator V1. During pulsed operation, the keyer normally conducts and keeps the klystron from oscillating. The negative pulse output of the width multivibrator cuts off the keyer, and the klystron oscillates for the duration of the input pulse.

*r. Klystron Oscillator V1*. The klystron oscillator circuit uses a SRU-55A type reflex oscillator tube and its associated plumbing to generate signals in the 16-kilomegacycles (kmc) ±250-megacycles (mc) range. By operating the OSCILLATOR TUNING control on the front panel, the spacing of the klystron resonator grids is varied to obtain the desired frequency. The klystron output may be a continuous-wave (cw), pulse-modulated (pm) or frequency-modulated signal, depending on the position of the MODULATION SELECTOR switch. In pulse or FM operation, the setting of the SYNC SELECTOR switch permits the application of internal or external triggering pulses. The time interval between the test set input triggering pulse and the initiation of the modulation pulse or the FM sawtooth wave is variable, by means of the DELAY control and the DELAY MULTIPLIER switch in the delay phantastron circuit. From the klystron oscillator, the signal is fed to the power set attenuator in the oscillator branch of the RF plumbing.

*s. POWER SET Control Attenuator AT3 and RF Shutter.* The power set attenuator control adjusts the output power of the klystron fed to the RF plumbing. The RF shutter is a waveguide switch that keeps the klystron signal from reaching the power monitor bridge and output attenuators when the FUNCTION SELECTOR switch is in the TRANS position. When the switch is in the RECV position, the klystron signal is unobstructed.

*t. Power Monitor Bridge.* The power monitor bridge is a temperature-compensated Wheatstone bridge used to measure the average power level of either RF output or RF input, depending on the position of the FUNCTION SELECTOR switch. The dynamic element of the bridge (a thermistor) is mounted in one branch of the RF plumbing.

*u. Fixed Attenuator AT1.* This fixed 6-decibel (db) attenuator is a section of waveguide mounted between the FUNCTION SELECTOR switch and the frequency meter.

*v. Frequency Meter Z2*. The frequency meter is an absorption-type meter used to measure the frequency of the RF output or RF input signal. It consists of a cavity that can be tuned by a knob ganged to the WAVEMETER FREQUENCY dial. The frequency meter is operated in conjunction with the power meter in the power monitor bridge circuit. The frequency to which the frequency meter is tuned is read directly from the WAVEMETER FREQUENCY dial.

*w. Rotary Attenuator AT2*. Klystron oscillator signals or external RF signals (fed in through the inputoutput waveguide) are attenuated by attenuator AT2. This variable attenuator is a section of waveguide mounted between an H-bend section of waveguide and the input waveguide section. The attenuator is actuated by the ATTENUATOR control knob on the front panel.

<span id="page-8-1"></span>*x. Input-Output Waveguide*. The input output waveguide consists of a length of waveguide with two branches terminator in three choke flanges. Energy

received by the test set is fed to the RF connector and travels down the input-output waveguide. A small portion of the energy is iris-coupled to the crystal detector. Energy transmitted by the test set passes out of the unit through the input-output waveguide and is available at the RF connector.

*y. Minus 300-Volt Power Supply*. A 105- to 125 volt, 50- to 420-cycle-per-second (cps) single-phase ac power source is required for operating the negative power supply. The direct current (dc) output of the rectifier is filtered and electronically regulated. A negative 300-volt output potential provides voltages for the thermistor bridge supply, all plate and screen circuits except the keyer, and the klystron resonator grids.

*z. Bias Supply*. The bias supply is regulated by type OA2WA bias voltage regulator V10. This -450-volt output potential is used to bias trigger generator V109, width multivibrator V110, trigger amplifier V103A, undelayed sync generator V103B, delayed sync generator V106A, and fm generator V108A. It is also used to supply the voltage for cathode follower V104A. In addition, the bias supply provides a reference voltage for the -300-volt supply.

*aa. Keyer (200-volt) Power Supply*. A 105- to 125 volt, 50- to 420-cps, single-phase alternating-current (ac) power source is required for the operation of the 200-volt keyer power supply. The 200-volt output is electronically regulated by a circuit consisting of negative series regulator tube V6B, dc amplifier V12, and negative voltage reference tube V13. The negative output, which is applied to the klystron reflector and keyer cathode, may be varied from -272 to -468 volts with respect to ground. The negative output, which is applied to the keyer plate, is at the same time varied with respect to ground from -172 to -268 volts. The potential applied to the keyer circuit is, therefore, always 200 volts. The potential applied to the reflector with respect to the klystron cathode is varied by the REFLECTOR control.

# <span id="page-8-0"></span>**Section II. UNIT THEORY**

# **3. Timing of Waveforms**

[\(fig. 2\)](#page-9-1)

<span id="page-8-2"></span>*a.* The time relationships between the significant waveforms produced in the test set circuitry are shown in [figure 2.](#page-9-1) External video pulses, sine waves, detected RF signals, or internally generated timing signals are used to synchronize the trigger generator (V101B and V102A) and to establish the repetition rate of the waveforms produced.

*b*. The input signal to the trigger generator is a train of negative pulses applied to the grid of V102A. The plate output of V102A is then differentiated and the negative pip is clipped. The positive pip applied to the grid of trigger amplifier V103A is used to trigger the undelayed sync generator and the delay phantastron; therefore, the undelayed video pulse at the UNDELAYED OUTPUT SYNC jack and the leading edge of the phantastron output pulse coincide in time with the input to the trigger generator.

*c*. The variable trailing edge of the phantastron output pulse at the screen grid of V105 is used to initiate the firing cycle of the circuitry that develops the delayed video pulse and the klystron keying pulse. This causes the delay video pulse at the DELAYED OUTPUT SYNC jack, the triggering pulse applied to the grid of the keyer trigger generator V109, and the leading edge of the keying pulse at the reflector of V1, during pulsed operation, to coincide in time.

*d*. The trailing edge of the phantastron output pulse also determines the firing cycle of the FM circuitry of the test set. Thus, the leading edge of the exponential waveform at the grid of delayed trigger amplifier V106B that is used to produce the FM triggering voltage for the FM generator, the leading edge of the FM trigger at the plate of delayed trigger amplifier V106B, and the beginning of the FM sawtooth voltage at the reflector of V1 coincide in time with the trailing edge of the phantastron output pulse.

## <span id="page-9-0"></span>**4. Crystal Dector**

[\(fig. 3\)](#page-10-0)

*a*. A type IN26 crystal detector mounted in a portion of waveguide acts as a detector of the RF power received from the input-output waveguide. The detected pulse output appearing at the cathode of the crystal detector is connected to connector J3 [\(fig. 4\)](#page-11-0) and is fed through cable W1 to the pulse amplifiers.

*b*. The crystal detector mount [\(fig. 3\)](#page-10-0) consists of a video filter and an RF choke. The RF input is fed into the detector by means of a waveguide-to-coaxial transformer (13) (shown in broken lines in [fig. 3\).](#page-10-0) This transformer provides a gradual tapering impendance match. At the end of the taper is a 1/4-wavelength transformer section (14). This section further reduces the dimensions of the waveguide to match the impedance of the guide to the impedance of the crystal. Therefore, the input RF signal is applied to the crystal without any appreciable loss of power. The RF is then picked up by the probe antenna (6) that forms part of the spring finger contact for one end of the crystal. From this point, the RF can go in two directions: either toward the video filter or toward the RF choke. The RF

encounters a near short circuit in the direction of the RF choke. In the opposite direction, provision is made for good RF coupling to the crystal by means of good contacts at both the inner and outer conductors of the coaxial crystal cartridge (10). The edge of the crystal



<span id="page-9-1"></span>*Figure 2. Timing waveforms.*

cartridge [\(fig. 3\)](#page-10-0) rests on a beveled seat having the same size opening as the inside diameter at the cartridge. The tip of the center pin slips into spring fingers cut in the end of a beryllium copper pin, insuring a tight fit. Because of this, the inner conductor of the coaxial line is continued to the inner conductor of the coaxial crystal. The outer conductor is pressed against the beveled seat by the crystal cap spring (12) inside the crystal cap (11). Good RF coupling at the seat is obtained by means of a choke. A noncontacting short continues from the outer conductor of the crystal cartridge to the outer conductor of the coaxial line; at the same time, it prevents RF leakage at this point. The choke consists of a low impedance 1/4-wavelength section (8) surrounding the crystal cartridge and a folded high impedance 1/4-wavelength section (9) surrounding the low impedance 1/4-wavelength section. This choke reflects a short at the point of contact between the crystal outer conductor and the mount The choke is backed up by a damping ring (7) of powdered iron to maintain the broadband characteristics of the detector. To prevent RF from entering the video line, a video filter is used. This filter consists of three sections of coaxial line: a section of low impedance, 1/4-wavelength long (5); a 1/4-wavelength section of much higher impedance (4); and a longer section filled with lossy powdered iron (3) which terminates the filter and provides high attenuation of the RF energy.

## <span id="page-10-1"></span>**5. Pulse Amplifiers V2 and V3**

## [\(fig. 4\)](#page-11-0)

*a*. When the SYNC SELECTOR switch S102 is placed in the EXT RF position, detected RF signals from the crystal detector [\(par. 4\)](#page-9-0) are amplified by two pulse amplifier stages (V2 and V3). Both stages use type 6AH6 pentode tubes and are very similar; with proper reference symbol substitution, the discussion of V2 also applies to V3.

*b*. When the SYNC SELECTOR switch is in the EXT RF position, -300 volts is a applied through S102A (V segment) to the cathode circuits of V2 and V3. Plate and screen grid resistors, R18 and R17, respectively are connected directly to ground which is the B+ connection of the -300-volt power supply. Resistor R21 and capacitor C4 are the decoupling network for V2; R20 and C23 decouple both stages from the power supply; capacitor C2 is the screen grid bypass capacitor; R19 is the cathode resistor. C3 is the cathode bypass capacitor, and L1 is a peaking coil.

*c*. The pulsed signal input from crystal detector CR1 is coupled to the control grid of V2 through shielded cable W1, capacitor C1, and parasitic suppressing resistor R14. The signal voltage is developed across diode load resistor R13. Resistor R16 is the grid return to cathode resistor. The output is coupled from the plate of V2 to the control grid of V3 through V5 and R22. The output of V3 is coupled through C7 and shielded cable W3 to the control grid of sync amplifier V101A.



- 1 BNC connector
- 2 Detected pulse output
- 3 Lossy termination
- 4 High impedance, 1/4-wavelength coaxial section
- 5 Low impedance, 1/4-wavelength coaxial section
- 6 Probe antenna
- 7 Damping ring
- 8 Low impedance, 1/4-wavelength choke section
- 9 High impedance, 1/4-wavelength choke section
- 10 Coaxial crystal cartridge
- 11 Crystal cap
- 12 Crystal cap spring
- <span id="page-10-0"></span>13 Waveguide-to-coaxial transformer
- 14 Quarter wavelength transformer section

*Figure 3. Crystal detector, cutaway view.*

#### **6. Sync Amplifier V101A**

#### [\(fig. 5\)](#page-12-0)

External triggering pulses, of negative or positive polarity, or sine waves are applied to the grid of V101A (pin 2) from INPUT SYNC jack J6 through shielded cable W2, jack 100, and capacitor C100. The positive pulse output of V3 [\(par. 5\)](#page-10-1) appearing at J101 is also applied to the grid of V101A. The signal voltage is developed across grid resistor R100. Resistor R101 is a parasitic suppressor and resistor R104 is the unbypassed cathode bias resistor. The plate load, consisting of parallel resistors R102 and R103, is connected to ground which is the B+ point of the -300 volt power supply. The output signal is taken from the plate of V101A through capacitor C101 and the wiper arm of SYNC SELECTOR switch S102B (Y segment). When the switch is -in the EXT RF or EXT POS position, the negative pulse output of V101A is applied to the grid of trigger generator V102A. When the switch is in the EXT SINE EXT NEG position, the positive pulse output of VIOLA is applied to the grid of trigger generator V101B. When a sine wave is applied to the INPUT SYNC jack,

either a sine wave or a square wave is applied to the grid of V101B, depending on the level of the input signal.

### **7. Rate Multivibrator V107**

#### [\(fig. 6\)](#page-13-0)

*a.* Rate multivibrator V107 is a free-running pule generator when SYNC SELECTOR switch S102 is set to either INT X 1 or INT X 10 position and MODULATION SELECTOR switch S103 is set to the PULSE or either of the FM positions. It provides triggering pulses at a pule repetition rate of 100 to 10,000 pps, depending on the position of SYNC SELECTOR switch S102 and RATE potentiometer R171A. When SYNC SELECTOR switch S102 is in EXT RF, SINE EXT NEG, or EXT POS, the cathode and grid line of V107A is opened by S102A (V segment) to remove -300 volts. When MODULATION SELECTOR switch S103 is in the CW position, the cathode and grid line V107A is opened by S103B (Y segment). When SYNC SELECTOR switch is in the INT X 1 position, the output frequency is between 100 and 1,000 pps, depending on the setting of the RATE control.



<span id="page-11-0"></span>*Figure 4. Pulse amplifiers schematic diagram.*

When S102 is in the INT X 10 position, the output frequency is between 1,000 and 10,000 pps, depending on the setting of the RATE control. The action of the rate multivibrator described in *b* and *c* below.

*b.* The grid (pin 2) of V107B is returned to it cathode (pin 3) through parasitic suppressor resistor R170, potentiometers R171A and R169. The grid (pin 7) of V107A is returned to -300 volts. The cathodes (pins 3 and 8) of V107 are connected together and returned to - 300 volts through cathode bias resistors R164 and R166. The voltage across R164 and R166 provides bias for V107A but does not provide bias for V107B. Consequently when -300 volts applied to the circuit, V107B begins to conduct more heavily than V107A.

*c.* When -300 volts applied to the circuit, both sections of the tube conduct, causing a voltage drop across resistors R164 and R166. The positive-going voltage across R164 and R166 increases the bias on V107A which causes a positive-going signal at the plate (pin 6) of V107A. The positive-going plate signal, resulting from the decrease in the potential drop across load resistor R167 is coupled through capacitor C117 or C118 and S102B (Z segment) to the grid (pin 2) of V107B. The positive going signal at the grid increases the current flow through V107B and increases the

voltage drop across its plate load resistor, R168; this produces a negative-going pulse at the plate (pin 1). At the same time, the increasing current through V107B increases the voltage drop across common cathode resistors R164 and R166. This increase in voltage across R164 and R166 further increases the bias applied to V107A, and a further decrease in V107A plate current results. The action is cumulative until V107A reaches cutoff. At this point, the voltage at the plate of V107A has reached ground potential and can no longer rise. Thus, the positive-going signal from the plate of V107A, impressed on the grid of V107B through either C117 or C118 is removed when capacitor C117 or C118 has charged to the same potential as the plate of V107A. Removal of the positive signal from the grid of V107B lowers the plate current through the tube and decreases the potential at its cathode and, therefore, at the cathode of V107A. This reduction of bias permits V107A to conduct. Conduction in tube V107A initiates a negativegoing voltage at its plate. The extent of the voltage drop at the plate is determined by the setting of R116, the 100 PPS ADJ potentiometer. This changing voltage is coupled through either capacitor C117 or C118 to the grid of V107B. Potentiometer R166 is an internal adjustment that is used to set the minimum rate



<span id="page-12-0"></span>*Figure 5. Sync amplifier, schematic diagram.*

(100 pps) of the multivibrator. The negative-going pulse at the grid of V107B decreases its plate current and, therefore, the potential across the common cathode resistors. As a result of this regenerative action, V107A conducts more heavily while the voltage at the grid of V107B goes well beyond the cutoff bias of the tube. The grid voltage is maintained beyond cutoff until capacitor C117 or C118 discharges sufficiently to allow V107B to conduct again. The rate of discharge is determined by the time constant network in the discharge path consisting of either C117 or C118 and R171A, R169, and the resistance of V107A. Potentiometer R169 is an internal adjustment that is used to set the maximum rate (10,000 pps) of the multivibrator. Potentiometer R171A is part of the RATE control and is used to vary the discharge rate of capacitor C117 or C118 to give a pulse repetition rate of either 100 to 1,000 or 1,000 to 10,000 pps, depending on the capacitor used. For each conducting period, a rectangular pulse of negative polarity is produced at the plate of V107B. This negative pulse is applied through SYNC SELECTOR switch S102A (X segment) and coupling capacitor C119 to the grid of trigger generator V102A [\(fig. 7\)](#page-15-0).

# **8. Trigger Generator V101B and V102A**

#### [\(fig. 7\)](#page-15-0)

*a*. The trigger generator, consisting of V101B and V102A, uses a Schmitt discriminator circuit to provide constant amplitude triggering pulses at a pulse repetition rate of 100 to 10,000 pps, depending on the pulse repetition rate of the input signal. The action of the trigger generator is described in *b* through *d* below.

*b*. Assume that SYNC SELECTOR switch S102 is in either the INT  $X$  1 or the INT  $X$  10 position and that the MODULATION SELECTOR switch is in the PULSE position. When −300 volts is applied to the circuit, V102A conducts heavily because its grid (pin 2) is returned to a more positive voltage than appears on the grid (pin 7) of V101B. The voltage on the grid of V102A is determined by the voltage divider network consisting of V101B plate load resistors R106 and R113 (in parallel with C102) and V102A grid resistor R114 The voltage on the grid of V101B is determined by the voltage divider network consisting of R111 and V101B grid resistor R112. The plate current of V102A, the heavily conducting tube, causes a voltage to be developed across common cathode resistors R107, R108, and R109. This voltage on the cathodes rises to such a



<span id="page-13-0"></span>*Figure 6. Rate multivibrator, schematic diagram.*

that the grid-to-cathode voltage on V102A is 0 volts. However, since the grid of V101B is returned to less positive voltage than the grid of V102A, the grid of V101B is negative with respect to the cathode and V101B is cut off. When a negative pulse output from the plate of rate multivibrator V107B is applied to the grid (pin 2) of V102A through S102A (X segment) and capacitor C119, the grid is driven below cutoff. Tube V102A plate current is cut off and the bias voltage for V101B developed across parallel cathode resistors R107, R108, and R109 is removed. The removal of the cathode bias from V101B causes the tube to conduct The plate current of V101B, flowing through plate load resistor R106, reduces the voltage at the plate of V101B. This lower voltage is coupled through voltage divider R113 and R114 to the grid of V102A. Therefore, a negative-going voltage appears at the grid of V102A; this reinforces the negative pulse originally received at that grid from the rate multivibrator. Tube V102A is already at cutoff and remains at cutoff for the duration of the input pulse. In this way, positive constant-amplitude pulses are developed across parallel plate load resistors R116, R117, and R118. Upon removal of the input pulse, the circuit is restored to its original condition. The positive pulses at the plate of V102A are coupled through capacitor C103 to the grid of trigger amplifier V103A. Capacitor C102 couples sudden changes in plate voltage of V101B instantly to the grid of V102A.

*c.* When switch S102 is in either the EXT RF or the EXT POS position, the action of the trigger generator is the same as explained in *b* above except that the negative triggering pulse fed to the grid of V102A comes from sync amplifier V101A through coupling capacitor C101 and S102B (Y segment).

*d*. When switch S102 is in the EXT SINE EXT NEG position, the action of the trigger generator is the same as that described for the INT X 1 and INT X 10 positions. If the external signal is negative, the resultant positive pulse is taken from the plate of V101A and fed through coupling capacitor C101 and S102B (Y segment) to the grid of V101B. The positive pulse of the grid of V101B causes the tube to conduct, producing a negative pulse at the plate. This pulse is coupled to the grid of V102A. If the external signal is a sine wave or a square wave, this signal is amplified and applied to the grid of V101B. Because V101B is normally cut off, the negative portion of the signal has no effect on the circuit. The positive

portion of the signal causes V101B to conduct, resulting in a negative pulse at the plate that is coupled to the grid of V102A. Therefore, whether the external signal is negative or a sine wave, the result is a negative pulse applied to the grid of V102A. This results in a trigger generator action similar to that described in *b* above.

# **9. Trigger Amplifier V103A**

## [\(fig. 8\)](#page-15-1)

*a*. The plate (pin 1) of trigger amplifier V103A and the plate (pin 6) of V103B are connected together and returned through the primary of transformer T101 to ground. The cathode (pin 3) is connected to the junction of cathode bypass capacitor C105 and cathode resistor R124. Capacitor C105 is connected to ground and R124 to the -300-volt supply. The grid (pin 2) is connected through crystal CR100 to the junction of the voltage divider network R121 and R122.

*b*. When MODULATION SELECTOR switch S103 is in the PULSE, FM X 1, or the FM X 10 position, resistors R121 and R122 form a voltage divider network between -300 volt and -450 volts through the Z segment of S103B. This causes V103A to bias slightly below the cutoff potential. The positive pulse output of trigger generator V102A is differentiated by coupling capacitor C103 and grid resistor R119. The negative peak of the differentiated wave is clipped by CR100, and the sharp, positive peak that remains is applied to the grid of V103A, driving it above the cutoff potential. The pulse appearing at the grid of V103A causes an amplified negative pulse to appear across the plate load impedance which consists of the primary of T101. The negative pulse at the plate (pin 1) of V103A is reversed in polarity and coupled by transformer T101 to the grid of undelayed sync generator V103B.

*c*. When MODULATION SELECTOR switch S103 is in the CW position, -300 volts is not applied to R121; therefore, -450 volts is applied to the grid. This causes V103A to bias well below the cutoff potential, and the positive pulse output of trigger generator V102A will not drive V103A above cutoff. During CW operation, the delayed and undelayed sync output pulses will not be produced.

#### **10. Undelayed Sync Generator V103B**

[\(fig. 9\)](#page-17-0)

*a.* Undelayed sync generator V103B uses a triggered blocking oscillator circuit to provide sharp pulses in either the PULSE, the FM X 1, or the FM X 10 position of the MODULATION SELECTOR switch. The repetition rate of the blocking oscillator is the same as that of either the internal rate multivibrator output or the



<span id="page-15-0"></span>*Figure 7. Trigger generator, schematic diagram.*



<span id="page-15-1"></span>*Figure 8. Trigger amplifier, schematic diagram.*

input sync pulse, depending on the setting o1 SYNC SELECTOR switch S102. When MODULATION SELECTOR switch S103 is in the CW position, there is no output from trigger amplifier V103A. The undelayed sync generator is cutoff because of the large negative bias or the grid (pin 7) applied from the -450 volt power supply. The action of the undelayed sync generator in all positions of the MODULATION SELECTOR switch except the CW position is described: in *b* through *d* below.

*b*. When power is initially applied to the circuit, a negative voltage from the bias supply is applied to the grid of the stage through the secondary of transformer T101 from a tap or the voltage divider consisting of resistors R127 and R129. Capacitor C106 is a bypass capacitor. The applied bas drives the grid beyond cutoff and, in the initial condition (before the application of a triggering pulse), the undelayed sync generator is not operative. The negative pulse from V103A is developed across the primary of transformer T101. The transformer reverses the polarity of the pulse, and the positive pulse applied to the grid of V103B is of sufficient amplitude to cause grid current to flow. The resultant current flow in the plate circuit causes a plate voltage drop that appears as a negative pulse across the primary winding of transformer T101. This action increases the negative voltage resulting from the applied trigger and, therefore, increases the positive voltage induced in the secondary of T101. This positive voltage is again impressed upon the grid of V103B and the cumulative action increases the level of conduction until saturation is reached. The voltage across the plate impedance can no longer increase and a voltage is no longer induced in the secondary of T101; therefore, the transformer magnetic field collapses. The grid (pin 7) voltage decreases and plate current is reduced. The decreasing plate current through the primary of T101 now induces in the secondary winding a negative potential signal that is applied to the grid of V103B, and cutoff is rapidly reached. During the time a positive voltage was applied to the grid, capacitor C106 charged to a small negative voltage. The values of R127 and C106 permit C106 to discharge in sufficient time for the blocking oscillator to be retriggered when the next driving pulse is applied.

*c*. The primary of transformer T101 and the distributed capacity across it constitute a tuned circuit. Because of the high Q of the circuit, shock-excited oscillations are produced at the end of the pulse. Resistor R123 is used as a damping resistor to reduce these oscillations.

*d*. During the conducting period, a positive pulse, with rise and decay times of less than 1-microsecond (μsec) duration, is developed across series cathode resistors R128, R126, and R124. This pulse is coupled from the junction of R128 and R126 through capacitor C116 to connector J104. Internal coaxial cable W102, terminated in mating connector P104, is connected from J104 to the front panel UNDELAYED OUTPUT SYNC jack J11. Pulses of approximately 1-μsec duration, with a minimum amplitude of 20 volts positive and with a repetition rate identical with the external o internal triggering pulse are available at jack J11 for application as trigger pulses to external equipment.

#### **11. Delay Phantastron V105, Cathode Follower V104A, and Clamp Diode V102B** [\(fig. 10\)](#page-18-0)

*a.* Delay phantastron V105 provides pulses of adjustable width at the repetition rate determined by the input pulse. The pulse width is variable from 1 to 1,000 μsec or up to 90 percent of the interval between triggering pulses, whichever is less. The maximum pulse width obtainable at 10,000 pps is 90 μsec. The phantastron output pulse repetition rate of 100 to 10,000 pps is identical with the repetition rate of the triggering pulses applied to its plate. The width depends on the position of DELAY MULTIPLIER switch S101 and the setting of DELAY potentiometer R132. When MODULATION SELECTOR switch S103 is in the CW position, trigger amplifier V103A is cutoff and no pulse appears at the plate (pin 5) to trigger delay phantastron V105. The action of the delay phantastron is described in *b* through *d* below.

*b*. With S103 in any position but CW, and S101 in the X1 position, V105 begins to conduct because its control grid (pin 1) is at a positive potential with respect to its cathode. The screen grid (pin 6) of V105 is connected to the voltage divider network consisting of parallel R143, R144, and R146 through R149. The screen grid (pin 6), control grid (pin 1), and cathode (pin 2) act as the normally conducting section of a multivibrator, with the screen grid corresponding to the plate and parallel resistors R143, R144, R146, and R147 serving as the plate load. The plate (pin 5), suppressor (pin 7), and cathode (pin 2) act as the normally cutoff section of a multivibrator; the suppressor acts as a control grid and is biased sufficiently negative to prevent the passage of electrons to the plate. Initially, the suppressor is at a negative potential with respect to the screen biased by voltage divider R136 and R137. The plate is connected to ground (B+ for the -300-volt power supply) through plate load resistor R138. Variations in the voltage applied to the suppressor have no appreciable effect on the total cathode current The suppressor, however, does control the division of current between screen grid and plate. In the initial condition of V105, the screen circuit is conducting and the plate circuit is cutoff. The positive pulse from the undelayed sync generator is coupled through C107 and crystal diode CR101 to the suppressor grid (pin 7) of delay phantastron V105. When the suppressor voltage is increased to that of the cathode voltage, plate current

begins to flow. This increase in plate current causes a drop in voltage at the plate of V105, the grid, and cathode of cathode follower V104A. The signal is coupled through C108 to the control grid of V105. The drop in grid voltage causes the cathode voltage to decrease. Hence, the suppressor voltage increases relative to the cathode voltage and more current is drawn by the plate. The plate voltage drops further and less current is drawn by the screen grid; this causes screen voltage to rise. The Miller rundown commences immediately after this regenerative action occurs.

*c*. The grid and cathode wave shapes of V105 are almost identical, because of the cathode follower. The initial plate voltage drop of V105 is the same as that of grid (V105) because they are connected together by C108. During the Miller rundown, the voltage across C108 is approximately equal to the plate-to-cathode voltage of V105. The discharge current of C108 is linear since the voltage across C108 cancels the plate-tocathode voltage of the delay phantastron, and is determined by grid and cathode resistors R141 and R139; therefore, the plate voltage of V105 is linear during the Miller rundown.



TM6625-228-35-9

<span id="page-17-0"></span>*Figure 9. Undelayed sync generator, schematic diagram.*

*d*. When the plate begins to draw current, the screen voltage initially rises because its current is reduced. During the rundown, its voltage remains approximately at the same level. Whet the plate voltage bottoms (is at a minimum), the grid voltage of V105 increases to the level of the cathode voltage with a time constant determined by the cathode follower output impedance and C108. The time constant is short because of the low output impedance of the cathode follower. Tube current and cathode voltage increase to cause the suppressor grid voltage to decrease relative to that of the cathode voltage. The plate current decreases to cause plate voltage to increase. The change in plate voltage is fed back through the cathode follower and C108 to the control grid to cause its voltage to rise still further. The action is regenerative and the circuit quickly returns to its original state.

*e*. The screen output is a pulse whose width can be controlled by DELAY potentiometer R132. The voltage level at which the rundown begins depends on the setting of this control: since V102 (clamp diode) causes the plate of V105 to be at the same potential as the center arm of R132 (pin 2) and therefore determines the time for the rundown to take place. MAX DELAY ADJ potentiometer R131 is adjustable so that a maximum delay of 100 microseconds can be attained. CR101 is used to prevent feedback between the delay phantastron and the undelayed sync generator. DELAY MULT ADJ R142 is set so that the delay will be multiplied by 10 in the X10 position.

*f*. Accordingly, DELAY potentiometer R132 is calibrated in microseconds. When DELAY MULTIPLIER switch is in either the X1 or X10 position, R132 sets the delay between 1 and 100 microseconds or 100 and 1,000 microseconds, respectively.

*g*. The output of V105 (screen) is differentiated by C109 and R151. Crystal CR102 clips the positive portion of the differentiated signal and the negative portion is applied to the grid of pulse amplifier V104B. The delay of this signal depends on the width of the pulse at the screen of the delay phantastron.

# <span id="page-18-1"></span>**12. Trigger Amplifier V104B and Delayed Sync Generator V106A**

[\(fig. 11\)](#page-19-0)

*a*. The plate (pin 6) of trigger amplifier V104B is connected to plate load resistor R152 and returned to ground (the B+ connection for the -300-volt power supply).



<span id="page-18-0"></span>*Figure 10. Delay phantastron, schematic diagram.*

The cathode (pin 8) is connected to -300 volts through cathode resistor R153. The positive input signal from the delay phantastron is differentiated by C109 and R151 and applied to the control grid of V104B. The positive portion of the differentiated signal is clipped by CR102 so that only the negative signal is amplified by V104B. The positive signal at the plate (pin 6) of V104B is coupled by C111 to the control grid of delayed sync generator V106A.

*b*. Delayed sync generator V106A is a triggered blocking oscillator circuit used to provide an output pulse with a repetition rate identical with the input trigger pule; the amount of delay time is determined by the width of the positive pule at the screen grid of delay phantastron V105. When MODULATION SELECTOR switch S103 is in any position but the CW position, the positive pulses from trigger amplifier V104B are fed through C111 to trigger delayed sync generator V106A. The operation of the delayed sync generator is described in *c* below.

*c.* When power is applied to this circuit, a negative bias is produced on the grid (pin 2) of V106A; this voltage is developed across R154 by the voltage divider network consisting of R154 and R163. The applied bias drives the grid below cutoff, preventing V106A from conducting. The positive pulse from trigger amplifier V104B drives the grid above cutoff and causes V106A to conduct. The resultant current flow in the plate (pin 1) circuit causes a plate voltage drop that appears as a negative signal across the primary of transformer T102. This signal appears inverted across the secondary of the transformer and therefore on the grid of V106A. This signal, therefore, adds to the positive signal on the grid of V106A. This cumulative action increases the level of conduction until saturation is reached. At this point, the magnetic field of the transformer collapses. The effect is again cumulative and V106A is quickly driven to cutoff. Resistor R156 is used to dampen any oscillations that may occur due to the transformer stray capacitance. Coincident with the negative plate pulse, a positive pulse is produced across cathode resistors R157 and R158. This pulse is coupled through R186 and C128 to keyer trigger amplifier V109 and through capacitor C115 to BNC connector J103. By means of internal coaxial cable W101, the positive pulse is available at front panel DELAYED OUTPUT SYNC jack J10. The negative signal at pin 3 of T1 is coupled through capacitor C114 to the control grid (pin 7) of trigger amplifier V106B. Capacitor C112 is the cathode bypass capacitor.



<span id="page-19-0"></span>*Figure 11. Trigger amplifier and delayed sync generator, schematic diagram.*

#### **13. Keyer Trigger Generator V109**

[\(fig. 12\)](#page-20-0)

*a.* The keyer trigger generator is a triggered blocking oscillator circuit similar to V106A. It develops the negative pulse required to trigger the width multivibrator. This stage uses a type 6CL6 pentode; the suppressor grid (pin 7) and cathode (pin 1) are connected to -300 volts. The plate (pin 6) is connected to ground through the primary winding (terminals 1 and 2) of blocking oscillator transformer T103. The screen grid is connected to ground. The control grid is connected through the secondary winding (terminals 3 and 4) of blocking oscillator transformer T103 to the voltage divider network consisting of resistor R184 and BIAS ADJ potentiometer R188. The two resistors are connected in series between -300 volts and -450 volts.

*b.* The circuit operates in all positions but the CW position of MODULATION SELECTOR switch S103 in the following manner: In the absence of a signal, the tube is maintained at cutoff by the negative potential on the grid. The positive pulse from delayed sync generator V106A is coupled to the grid through resistor R186, capacitor C128, and the secondary of T103, and causes the tube to conduct. The resultant plate current flows through the primary of transformer T103 and causes the plate voltage to fall. The falling potential appearing across the plate impedance is coupled through T103 to the grid as a positive rising potential. This positive

voltage on the grid causes a further increase in plate current The action is cumulative until plate current saturation is reached. At this point, the current through the plate circuit can no longer increase and the field in the primary remains constant. Therefore, the positive potential across the secondary de-creases. With the decrease of plate current through the primary, a voltage is induced in the secondary that applies to negative potential to the grid. Plate current cutoff is quickly reached. The tube is held at cutoff until the next positive pulse arrives from the delayed sync generator to trigger the blocking oscillator.

*c*. During the conduction period, a narrow negative pulse is produced at the plate and fed through crystal CR104, PULSE WIDTH potentiometer R194, and capacitor C132 to the grid of one-half width multivibrator V111. Resistor R190 is connected across the primary of T103 to dampen ringing for more than 1/2-cycle.

#### **14. Width Multivibrator V110 and V111**

[\(fig. 13\)](#page-22-0)

*a.* Two type 6CL6 power pentodes, V110 and V111, are connected as a monostable multivibrator stage. The plate (pin 6) of V110 is connected through resistor R191 in parallel with potentiometer R194 and resistor R193 to ground. The plate (pin 6) of V111 is connected through parallel resistors R201 and R202 to ground.



<span id="page-20-0"></span>*Figure 12. Keyer trigger generator, schematic diagram.*

The suppressor grid (pin 7) and the cathode (pin 1) of each tube are connected to -300 volts. The control grid (pins 2 and 9) of V111 is maintained at a more positive potential than the cathode through dropping resistor R199 and WIDTH ADJ potentiometer R198. The control grid of V110 is maintained at a more negative potential than the cathode through grid return resistor R196. It is connected to the voltage divider network consisting of resistors R189 and R192 which develops the grid bias. Capacitor C131 is the bypass capacitor. Parallel resistors R204 and R206 in series with R203 form a voltage divider network to which the screen grid of V111 is connected. Capacitor C134 is the screen grid bypass capacitor.

*b.* The circuit operates in all positions except the CW position of MODULATION SELECTOR switch S103 in the following manner: In the absence of a triggering voltage, V111 is normally conducting, and V110 is cut off by the negative potential on its grid The negative pulse from keyer trigger generator V109 is applied through crystal CR104, PULSE WIDTH control R194, and capacitor C132 to the grid of V111 and causes a positive pulse of voltage at the plate This positive pulse at the plate is coupled through capacitor C133 to the control grid of V110 and drives the grid voltage of this tube momentarily above cutoff. When V110 conducts, the plate voltage drops. This change of voltage is coupled to the grid of V111 through C132. This is a regenerative process which drives V111 to cutoff. However V1111 cannot remain cutoff, because its grid is returned through R199 and R198 to ground while its cathode is returned to -300 volts. As capacitor C132 discharges, the grid voltage of V111 rises exponentially. As soon as the rising grid voltage reaches the cutoff level V111 begins to conduct again, a second switching action occurs, and the normal condition (V111 conducting and V110 cutoff) is re-established. This conduction remains until another trigger pulse is applied. Conduction occurs in the screen grid of V110, when the plate conducts, and causes a drop in the screen grid voltage The negative pulses that appear at the plate and screen of V110 are timed by trigger pulses from keyer trigger generator V109. The leading and lagging edge of the negative pulse appearing at the screen of V110 is peaked by peaking coil L100. Crystal CR105 is connected across R197 (the screen load resistor) and L100 to dampen the screen grid overshoot.

*c*. The width of the negative output pulses form the screen. grid circuit of V110 may be adjusted by the front panel PULSE WIDTH control from .2 to 2 microseconds. Potentiometer R194 controls the amount of negative pt voltage change (V110) that is applied through C132 to the control grid of V111. The time required for C132 to discharge sufficiently to bring V111 out of cutoff, after the initial application of the negative pulse, is determined by the setting of R194 and WIDTH ADJ potentiometer R198 in the capacitor discharge path. When V11 cuts off, V110 conducts and the negative pulse is produced in the screen grid circuit of V110. When V111 is driven above cutoff, V110 is cut off and terminates the negative pulse in the screen grid circuit. Initially, the PULSE WIDTH control is set to the 2.0 position (maximum signal applied through C132 to V111 grid) and the WIDTH ADJ potentiometer is adjusted to produce a V110 screen grid circuit output pulse 2 microseconds wide. Thereafter, changing the setting of the PULSE WIDTH control changes the width of the output pulses. The output pulses from V110 are fed to keyer V112 through coupling capacitor C135. Resistor R195 is a parasitic suppressor.

# **15. Keyer V112**

[\(fig. 14\)](#page-23-0)

*a.* Keyer stage V112 uses a type 6CL6 pentode triode-connected in a cathode follower circuit. The plate (pin 6) is supplied from the positive side of the keyer supply through parallel dropping resistors R211 through R213. Capacitor C137 serves as a plate bypass. The cathode (pin 1) is connected to the -372-to -468 volt reflector supply through parallel cathode resistors R214, R216, and R217. The grid (pins 2 and 9) is connected through R208, grid return resistor R207, and AM ADJ potentiometer R209 to the cathode (pin 2) of V13. The cathode of V13 is maintained 150 volts more positive than the reflector supply. Resistor R208 is a parasitic suppressor. AM ADJ control R209 is used to vary the grid bias of V112 and, therefor the voltage drop across the parallel cathode resistor. The keyer acts as a transitional stage between the modulator section and the klystron.

*b.* When MODULATION SELECTOR switch S103 is in the CW position, the reflector voltage at pin 5 of RF oscillator V1 is obtained through R172 from the -372- to - 468-voltage reflector supply, and the klystron produces continuous wave (cw) oscillations. When S103 is in the PULSE position, the strong reflector voltage is taken from the parallel cathode resistors. This voltage is adjusted, by AM ADJ potentiometer R209, to be 40 volts more positive than the reflector voltage with S103 in CW position. This difference in the voltage applied to the reflector causes the klystron to be outside the reflector mode, and the klystron will not oscillate. When a negative pulse from-the width multvibrator appears at the grid of the keyer, the keyer is cut off. With the keyer cut off, there is no voltage drop across the cathode resistors and the -372- to -468-voltage of the reflector supply is available at the cathode. With the application of this voltage, the klystron reflector is restored to the center of its operating mode. The klystron oscillates for the duration of the pule applied to the keyer and thus is pulsed to a cw level. The extent to which the klystron is shifted from the center of its operating mode is determined by the adjustment of AM ADJ potentiometer

R209. Both the cw reflector voltage and the keying voltages for pulse operation are coupled by the wiper arm of MODULATION SELECTOR switch S103A (V segment) to the reflector (pin 5) of the klystron. Resistor R172 prevents shorting of the keyer cathode load when the switch is rotated from one position to another. Capacitor C136 bypasses AM ADJ potentiometer R209.

### **16. Trigger Amplifier V106B**

[\(fig. 15\)](#page-24-0)

Tube V106B and its associated circuitry is used as a clipping amplifier in which the grid (pin 7) is returned to ground through grid return resistor R162. The negative exponential voltage from the delayed sync generator [\(par. 12\)](#page-18-1) is coupled by capacitor C114 to the grid of V106B. The steep wave front of the sawtooth quickly drives the tube that is normally conducting to cut off. Plate current drops to zero and remains there while the grid is below cutoff. The grid rises exponentially as capacitor C114 starts to discharge toward ground. When the grid voltage reaches the cutoff value, V106B



<span id="page-22-0"></span>*Figure 13. Width multivibrator, schematic diagram.*

conducts for the remainder of the exponential rise. Thus, a positive pulse is produced at the plate load consisting of parallel resistors R159 and R161. This positive pulse is coupled by capacitor C126 to the grid (pin 2) of FM generator V108B.

### **17. FM Generator V108B**

#### [\(fig. 15\)](#page-24-0)

*a*. FM generator V108B develops the frequencymodulating voltage for the klystron in FM operation. Normally, V108B is cut off by the large negative bias on its grid obtained from voltage divider network R182 and R183 connected between the -300-volt and -450-volt supply. Capacitor C125 is the bypass capacitor.

*b*. When the positive pulse from the trigger amplifier is applied, V108B conducts heavily. The voltage drop across plate load resistors R179 and R171B causes either capacitor C121 or C122 to discharge through section A (X segment) of MODULATION SELECTOR switch S103 and V108B. Depending on the FM position (FM X 1 or FM X 10) of switch S103, either capacitor C121 or C122 is then charged through resistor R179 and RATE control

R171B. When V108B is cut off, the voltage across these capacitors rises exponentially, until the next trigger from V106B discharges either capacitor. The amplitude that either capacitor discharges to depends on the trigger rate and the charging time constant. The generated sawtooth is coupled by capacitor C123 to the grid (pin 7) of FM amplifier V108A. RATE potentiometer R171B in the plate circuit of V108B is ganged with R171A in the grid circuit of the rate multivibrator to coordinate the charging time with the trigger rate, so that a sawtooth of good linearity and approximately constant amplitude is produced. Resistor R181 is the grid return resistor.

### **18. FM Amplifier V108A**

#### [\(fig. 15\)](#page-24-0)

The amplifier stage for the FM sweep voltage is a conventional RC-coupled triode amplifier. Capacitor C123 is the coupling capacitor. FM AMPLITUDE potentiometer R174, in the grid circuit varies the amplitude of the sawtooth applied to the grid of V108A and therefore the klystron repeller plate for FM operation.



<span id="page-23-0"></span>*Figure 14. Keyer and klystron oscillator, schematic diagram.*

This determines the limits of the frequency deviation from the center frequency. The amplified and phaseinverted signal appearing at plate load resistor R176 is coupled by capacitor C124 to pins 3 and 4 of MODULATION SELECTOR switch S103A (V segment). Cathode bias for V108A is provided by resistor R177.

#### **19. Klystron Oscillator V1**

#### [\(fig. 16\)](#page-25-0)

The equipment, when used as a signal generator, produces an RF signal of known and adjustable frequency and power level. This signal is generated by V1, a velocity-modulated type SRU-55A klystron used as a reflex oscillator. Oscillations are produced as follows:

*a*. The tube elements consist of a reflector electrode (pin 5), resonator grids (pin 1), and a cathode (pin 8). The cathode is at -300 volts, the resonator grids are at ground potential, and the reflector voltage is obtained from the negative reflector supply through MODULATION SELECTOR switch S103A (V segment). When S103 is in the CW position -372 to -468 volts is obtained through resistor R172. When S103 is in the PULSE position, reflector voltage is obtained from the

cathode of keyer tube V112. When S103 is in the FM positions, reflector voltage is obtained from the plate of FM amplifier V108A.

*b*. The electron gun produces a focused electron beam of uniform velocity. A re-entrant cavity resonator, tunable by varying the spacing of the resonator grids and the volume of the resonator cavity, is an integral part of the tube. A varying RF field exists between the resonator grids, and a strong negative field exists between the reflector electrode and the resonator grids. The RF field is generated when the cavity is shocked into oscillation by the initial surge of current when voltage is applied to the tube. The varying RF field acts on the electron beam as it passes the resonator grids. The RF field slows up those electrons arriving when the grid nearest the reflector is negative with respect to the grid nearest the cathode and speeds up those electrons passing when the grid nearest the reflector is positive with respect to the grid nearest the cathode. Other electrons pass the grids at an intermediate speed when both grids are at the same potential. This process is known as velocity modulation. After the electrons pass



<span id="page-24-0"></span>*Figure 15. Trigger amplifier, fm generator, and fm amplifier, schematic diagram.*

the grids and approach the reflector, they come under the influence of the negative field existing between the reflector and the grids and are repelled back toward the grids. The faster an electron is traveling when it passes the grids, the closer it will come to the reflector plate, and the greater will be its speed when it is repelled back to the grids. Because of this action, the slower moving electrons are overtaken by the medium speed electrons. These electrons group together and are in turn overtaken by the faster moving electrons. In this way, all the electrons that pass the grids during a given cycle are bunched as they approach the grids on their return from the reflector plate area. The reflector voltage is adjusted so that the bunches of electrons return to the grids when the grid nearest the reflector is positive with respect to the grid nearest the cathode. The bunched electrons are slowed down in the area between the grids. The energy is then taken from the bunches and delivered to the resonator cavity.

*c.* RF energy is taken from the resonator cavity and injected into the radar test set plumbing by means of aperture-coupling between the klystron cavity and the waveguide.

*d.* The frequency of oscillation is determined by the spacing of the resonator grids. Decreasing the distance between the grids increases the capacitance of the resonator cavity and thereby decreases the natural frequency of oscillation. Test jack J12 is provided to measure klystron current.

#### **20. Power Set Attenuator AT3**

#### [\(fig. 17\)](#page-26-0)

Power set attenuator AT3 is a waveguide type attenuator inserted between the klystron and the FUNCTION SELECTOR switch. It attenuates RF energy in the  $TE_{1,0}$  mode over the frequency range of 12.4 to 18.0 kilomegacycles. In this mode, the electric field strength increases from zero at the side of the guide to maximum at the center. Attenuation is effected by the



<span id="page-25-0"></span>*Figure 16. Klystron oscillator, schematic diagram.*

movement of a resistance card from the top to the bottom of the guide. The loss caused by the attenuator that lies parallel to the electrical field increases as the resistance card is displaced toward the bottom of the guide. This insertion provides 0-to 40-db attenuation of the klystron power output so that a power reference level of 1 milliwatt may be established for any level of kystron power output. The mechanical operation of the attenuator may be understood by referring to [figure 17.](#page-26-0) Rotation of a cam by a shaft causes the card to move up or down.

#### **21. Power Monitor Bridge**

#### [\(fig. 18\)](#page-28-0)

The power monitor bridge uses a Wheatstone bridge circuit in which a bead thermistor constitutes one arm of the bridge. The bead thermistor (RT2) is connected across a branch of the RF plumbing so that it will absorb RF input or output power, depending on the mode of operation. The circuit also incorporates two disk thermistors: RT1 and RT3. Thermistor RT3 is used for temperature compensation and RT1 is used for zero drift compensation. The disk thermistors are mounted on either side of the thermistor mount branch of the RF plumbing to compensate for changes in temperature and bridge sensitivity. The disk thermistors have relatively large mass and their resistance is varied by the ambient temperature. Although the thermistors are physically located in the RF plumbing as shown in section A, electrically they form part of, and are connected to, the



<span id="page-26-0"></span>*Figure 17. Power set attenuator, cutaway view.*

actual Wheatstone bridge circuit This relationship is indicated in section B by showing the thermistors connected in the actual bridge circuit, However, their outlines are dotted to indicate that they are housed in the plumbing.

*a.* The basic Wheatstone bridge circuit consists of resistors R2, R6, and R7 and thermistor RT2. When the bridge is balanced, no current flows through meter M1 connected across two arms of the bridge. Balance is obtained when the resistors in the circuit satisfy the following equation:

$$
Resistance of RT2 = R2 X
$$
\n
$$
RT2 = R2 X
$$
\n
$$
RT2 = R2 X
$$

The resistance of a thermistor varies inversely with the current through it, or the ambient temperature. The first of these thermistor characteristics is used to obtain bridge balance. Voltage regulator tube V8 maintains the voltage applied to the bridge from the -300-volt supply at -108 volts. When voltage is applied to the bridge, the current through thermistor RT2 causes a change in its resistance. The current required to vary the resistance of the thermistor to the proper value is controlled by the front panel ZERO SET control. This control front panel ZERO SET control. (potentiometer R10) varies the voltage applied to the bridge and hence the current through the thermistor. During operation, the control is adjusted to cause the resistance of the bead to satisfy the equation shown above. When all resistances are equal, the bridge is balanced. and no current flows through the meter. COARSE ZERO SET ADJ potentiometer R11 permits further adjustment of the thermistor current if it cannot be adjusted sufficiently with the ZERO SET control.

*b*. The ability of the thermistor to change Its resistance through absorption of the RF power is made use of to provide a 1-milliwatt reference level for RF output power measurements. Assuming that the bridge has been balanced in CW operation, RF power applied to the bead thermistor connected across the waveguide would cause the bridge to become unbalanced and current to flow through the meter. The change is resistance of the thermistor is approximately linear with respect to the amount of applied RF power. Consequently, the meter scale is calibrated linearly to

indicate output power in milliwatts or in db referenced to 1 milliwatt (dbm). Midscale on the milliwatt scale represents the 1-milliwatt level or 0 dbm. To set the 1 milliwatt level, once the bridge has been balanced, the POWER SET control on the front panel, which controls a waveguide attenuator, is rotated until the meter needle deflects to midscale. In measuring input power, the power set attenuator is blocked off from the main waveguide. The rotary attenuator is adjusted to cause a midscale or power-set deflection of the meter and the strength of the input signal is read in db above 1 milliwatt on the + scale of the POWER DBM dial.

*c*. In addition to the basic thermistor power bridge circuit the power monitor bridge incorporates compensative devices for changes in temperature and sensitivity.

(1) The thermistor bridge tends to increase in sensitivity with a decrease in temperature. The sensitivity in ohms-per-watt of the thermistor bead remains constant over a broad temperature range, but the bridge sensitivity (in microamperes meter reading per milliwatts of RF power) increases with a decrease in temperature. As the temperature goes down, the thermistor resistance tends to go up, making it necessary to apply a higher voltage to the bridge by adjusting the ZERO SET control. Because of this higher voltage, the change in current through the meter, due to a given change in thermistor resistance, is greater at lower temperatures. Compensation for this variation in sensitivity is made by increasing the meter resistance as the temperature decreases. Since a disk thermistor increases in resistance with decrease in temperature, one is placed in series with the meter. In addition, it is necessary to place resistor R1 in parallel with thermistor RT3 and R3 or R4 in series with the R1-RT3 combination to obtain the correct rate of change of resistance with temperature. Thus, the sensitivity of the bridge remains constant over the required temperature range. When FUNCTION SELECTOR switch S2 is in RECV position, R3 is

adjusted so that with a known power output of 1 milliwatt (mw) and with the rotary attenuator set at 0 dbm (actually has a 6-db drop at this point) the meter reads CAL. In TRANS position, R4 is similarly adjusted with a known power input of  $+6$  dbm and the rotary attenuator set at +6 dbm. (Actually, it should have a 0-dbm drop at this point.) However, the rotary attenuator has a 1-db insertion loss. To correctly calibrate the bridge in TRANS position, R4 is made smaller than R3.

(2) To eliminate the frequent resetting of the ZERO SET control, automatic provision is made for increasing the current through the bead thermistor with a decrease in temperature. Disk thermistor RT1, the resistance of which increases with decreasing temperature, is put in parallel with the bridge. More current flows through the bridge at lower temperature because the ratio of the resistance of the shunting disk thermistor to the resistance of the bridge (between points A and B [\(fig. 18\)](#page-28-0) is greater at lower temperature. To adjust this compensation to cover the required temperature range, the thermistor is combined in a network with resistors R8 and R9.

*d*. The meter is used in frequency measurements because the frequency meter, when tuned to resonance, causes a sharp deflection of the meter pointer.

## **22. Frequency Meter Z2**

#### [\(fig. 19\)](#page-29-0)

Frequency meter barrel is coupled to a T-section of waveguide that connects the assembly to the fixed attenuator AT1 and thermistor mount Z1. Tuning of the cavity is accomplished by means of a noncontacting plunger shaft ganged to a direct reading dial on the front panel. When the cavity is tuned to resonance for the incoming or outgoing RF signal, the cavity absorbs energy, causing a decrease in power at the thermistor bridge and a corresponding dip of the power meter needle. When the FUNCTION SELECTOR switch is in

the RECV position, half of the klystron output passes the frequency meter on its way to the thermistor mount In the TRANS position, the klystron output is obstructed by means of an RF shutter or waveguide switch that is inserted across the waveguide, and the frequency meter measures only the frequency of the incoming RF. The RF shutter contains a pin which shorts out the E field in the oscillator line and acts a continuous path for the current in the main guide. The pin is withdrawn in the RECV position and is fully inserted in the TRANS position.

## **23. Rotary Attenuator AT2**

[\(fig. 19\)](#page-29-0)

The output attenuator is a waveguide type attenuator designed to attenuate RF energy in the  $TE_{1,0}$  mode over a frequency range of 12.4 to 18.0 kilomegacycles. The attenuator provides 0 to -90 dbm of calibrated attenuation. In this mode, the electric field strength increases from zero at the side of the guide to maximum at the center. Attenuation is affected by the rotation of the metalized mica vanes and can be shown as follows for one-half of the attenuator:

*a*. The location of the vanes in respect to each other will have an attenuation of 0 db as shown in A, B,

and C, [figure 61.](#page-74-0)

*b*. When the vane is rotated, the relations between the vanes and the electric field are as shown in D, E, and F, [figure 61.](#page-74-0)

*c.* The component of the electric field that is not attenuated is:

$$
E_1 = E \text{ Cos } B \text{ and } E_2 = E_1 \text{ Cos } B.
$$

Therefore, the output of one half of the attenuator is  $E_2$ =  $E \cos^2 B$ . Expressed in *DB*, it will be  $A = 20$  log  $\cos^2 B$ or *A* = 40 log Cos *B*. This indicates that the attenuation increases as B goes from 0° to 90°. The mechanical operation of the attenuator may be understood by referring to [figure 19,](#page-29-0) a cross-sectional view. Rotation of the shaft with a worm gear drives two worm follower gears, which rotate the metalized mica vanes in the electric field.

#### **24. Fixed Attenuator ATI**

[\(fig. 28\)](#page-41-0)

The dbm attenuator is a waveguide type designed to attenuate RF energy over the frequency range of 12.4 to



<span id="page-28-0"></span>*Figure 18. Power monitor circuit schematic diagram.*

18.0 kilomegacycles. The attenuator provides 6 db of calibrated attenuation. It is a side wall attenuator, where a card is placed in such a direction that the plane of the card lies in the same plane defined by the electric field and the direction of propagation. The card is placed at such a distance from the side wall that an attenuation of 6 db is achieved.

## **25. Keyer Supply, 200 Volts**

#### [\(fig. 20\)](#page-30-0)

The keyer supply is a regulated power supply that furnishes the keyer voltages and the klystron reflector voltage and uses a type 5Y3WGTA tube (V11) a fullwave rectifier. One half of a type 6080WA dual triode (V6B) is used as a series regulator and a type 5751 dual triode (V12) functions as a dc amplifier.



<span id="page-29-0"></span>*Figure 19. RF waveguide system, cutaway view.*

A type OA2WA voltage regulator tube (V13) serves as a voltage reference tube. The circuit functions as follows:

*a*. The ac voltage applied to the plates (pins 4 and 6) of V11 from taps 3 and 5 of the secondary of transformer T2 is rectified by the tube. Tap 4 is the center tap of the plate winding. The rectified voltage from pin 2 is filtered by capacitor C15. The filtered dc appears at the plate (pin 5) of V6B. At the cathode (pin 6) of V6B, there is -172- to -268-volt output that is positive with respect to the -372- to -468 reference voltage; the regulation is accomplished as follows: The grid (pin 4) of V6B is connected to the plate (pin 1) of dc amplifier V12. The voltage at the grid of V6B is controlled by the voltage at the plate (pin 1) of V12. Resistors R52 and R54 are the plate load resistors for V12A and V12B, respectively. Resistors R58 and R61 and potentiometer R59 constitute a bleeder across the output. The grid (pin 7) of V12 is connected through R57 to the wiper arm of 200V ADJ R59. Because the cathodes (pins 3 and 8) are maintained at a fixed voltage determined by voltage reference tube V13, voltage variations in the output of the supply appear on the grid (pin 7) of V12. These changes are amplified by both sections of V12 and applied to the grid (pin 4) of the series regulator. This changes the voltage drop across series regulator tube V6B and restores the supply output to its designated level.

*b.* The circuit provides a -172- to -268-volt supply at the positive end of the bleeder. This voltage is fed to the plate load of keyer V112 [\(fig. 14\).](#page-23-0) At the same time, a negative voltage of -372 to -468 volts at the negative end of the bleeder is fed to the cathode of keyer V112. This negative voltage continues through S103C to the klystron reflector.

*c*. The other components of the V6B circuit include parasitic suppressor R51. Parallel resistors R62 and R66 in series with R64 and R63 constitute a voltage divider network across the output. Capacitors C19 and C21 are bypasses for REFLECTOR control R64 which



<span id="page-30-0"></span>*Figure 20. Keyer supply, 200 volts, schematic diagram.*

varies the voltage applied to the reflector. Capacitor C17 is a bypass for voltage reference tube V13. Capacitor C18 is a bypass for the 120-pps ripple frequency. Resistor R55 is used for discharging C15 when the set is turned off. Capacitor C16 is a high frequency bypass capacitor. DC7 and R35 couple dc voltage between V12A and V12B.

## **26. Minus 300-volt Supply**

[\(fig. 21\)](#page-32-0)

*a.* The -300-volt supply is a regulated power supply that furnishes the voltages for all the circuits except the keyer stage. Dual triode V5 and triode V6A are the series regulators for full-wave rectifier V4. Dual triode V7 is the dc amplifier.

*b.* The ac voltage applied to the plates (pins 4 and 6) of V4, from taps 3 and 6 of the secondary of transformer T1, is rectified by the tube. Tap 5 is the center tap of the plate winding. The rectified voltage from pin 8 is filtered by capacitor C9. The filtered dc voltage appears at the plates (pins 2 and 5) of V5 and the plate (pin 2) of V6A. At the cathode (pin 8) of V7 a -300-volt output is produced; the regulation is accomplished as follows.

*c.* A reference voltage of 450 volts is applied to the voltage divider network consisting of resistors R47, R48, and R49. Should the output voltage change to a greater value than -300 volts, a less negative voltage will be applied to the grid (pin 7) of V7. The dc voltage on the plate (pin 6) and cathode (pin 3) of V7 changes to a more negative value which is then coupled to the grids of the series regulator tubes V5 and V6A. The resistance of V5 and V6A increases causing the output voltage to be restored to the normal -300-volt level. Should the - 300-volt output voltage decrease in value, a less negative voltage will be coupled by V7 to the control grids of V5 and V6A. The resistance of V5 and V6A will decrease causing the -300-volt output voltage to be restored to the normal -300-volt level. Regulation will maintain the voltage determined by the setting of the -300V ADJ control.

*d.* Resistors R44, R31, and R32 are plate load resistors of dc amplifier V7. Capacitor C10 is the bypass capacitor. Resistors R33, R38, and R37 are parasitic suppressors for the grid circuit of the series regulators. Resistors R47, R49, and -300V ADJ control R48 form a voltage divider between ground and the -450-volt reference, and resistors R42 and R43 form a voltage divider. Resistor R46 and capacitor C13 serve to bypass the 120-cps ripple frequency. Capacitor C14 is a filter for the -300-volt supply. Resistors R34, R39, and R36 are cathode parasitic suppressors for the series regulator. Resistor R30 serves to discharge filter capacitor C9 when the test set is turned off. Tube V8 is used to supply -108 volts to the power monitor bridge. Capacitor C20 is used to dampen any oscillations produced by V8. Resistor R50 and V8 form a voltage divider network which provides -108 volts to the power monitor bridge circuit.

## <span id="page-31-0"></span>**27. Bias Supply**

[\(fig. 22\)](#page-32-1)

<span id="page-31-1"></span>The bias supply is a regulated power supply that furnishes -450 volts for bias purposes and supplies a reference voltage for the -300-volt supply. Dual plate V9 is connected as a half-wave rectifier. Regulation is provided by miniature voltage regulator V10. The circuit functions as follows: The ac voltage applied to the cathode (pin 7) of V9 from tap 4 of the secondary of T1 is rectified by the tube. The dc output appearing at the plates (pin 1 and 6) is fed to a pi-type RC filter network consisting of resistor R41 and capacitors C11 and C12. The filtered dc appears across the plate to the cathode of V10 and causes the gas to ionize and the tube to draw current. The glow tube current assumes the proper magnitude so that the voltage at the output is -450 volts. Any change in input de or load current is compensated for by an appropriate change in glow tube current while its voltage remains constant. Thus, within current limits, the -450-volt output is maintained.



<span id="page-32-0"></span>*Figure 21. Minus 300-volt supply, schematic diagram.*



<span id="page-32-1"></span>*Figure 22. Bias supply, schematic diagram.*

AGO 2704A

#### <span id="page-33-0"></span>**CHAPTER 2**

### **TROUBLE SHOOTING**

#### <span id="page-33-1"></span>**Section I. GENERAL TROUBLESHOOTING TECHNIQUES**

<span id="page-33-2"></span>*Warning:* **When servicing the test set, be extremely careful because of the high voltage present. Always be sure that the power cable is not plugged into the POWER INPUT connector when removing the test set from its carrying case. Discharge the capacitors in the power supply circuits before touching any parts.**

#### **28. General Instructions**

Troubleshooting at field and depot maintenance level includes all the techniques outlined for organizational maintenance and any special or additional techniques required to isolate a defective part. The field maintenance and depot procedures are not complete in themselves but supplement the procedures described in TM 11-6625-228-12. The systematic troubleshooting procedure, which begins with the operational and sectionalization checks that can be performed at an organizational level, must be completed by means of sectionalizing, localizing, and isolating techniques. [Paragraphs 31](#page-35-2) through [36](#page-45-0) describe techniques that must be performed at the field maintenance level.

#### **29. Troubleshooting Procedures**

*a. General.* The first step in servicing a defective test set is to sectionalize the fault. Sectionalization means tracing the fault to a chassis or circuit responsible for abnormal operation. The second step is to localize the fault. Localization means tracing the fault to the stage within the chassis or circuit responsible for abnormal operation. The third step is to isolate the fault. Isolation means tracing the fault to a defective part responsible for the abnormal condition. Some faults, such as burned-out resistors and arcing and shorted transformers can often be located by sight, smell, and hearing. The majority of faults, however, must be isolated by checking voltages and resistances.

*b. Sectionalization.* The test set consists of several groups of circuits on two separate chassis; the main chassis and the modulator chassis. The first step in tracing trouble is to locate the circuit or circuits at fault by the following methods:

- (1) *Visual inspection.* The purpose of visual inspection is to locate faults without testing or measuring circuits. Readings of the meter or other visual signs should be observed and an attempt made to sectionalize the fault to a particular chassis or circuit.
- (2) *Operational tests.* Operational tests frequently indicate the general location of trouble. In many instances, the tests will help in determining the exact nature of the fault. The equipment performance checklist in TM 11-6625-228-12 is an operational test. Additional operational tests are given in [paragraph 32.](#page-36-0)

*c. Localization.* After the trouble has been sectionalized, use the tests listed below as an aid to localize the trouble. This procedure will localize the trouble to a portion (usually a stage) of the system or chassis.

- (1) *Stage-gain measurements.* The stagegain figures given in [paragraph 33](#page-39-0) will help to locate hard-to-find troubles in the pulse-amplifier stages.
- (2) *Signal substitution.* Signal substitution procedures for the pulse amplifiers [\(par. 33\)](#page-39-0) help the repairman to localize a trouble quickly to a stage. Pulse Generator AN/UPM-15 and Oscilloscope USM-50 are units of test equipment that may be used in signal substitution procedures.

*d. Isolation.* After the trouble has been localized to a portion (usually a stage) of the system or chassis, use the tests listed below as an aid to isolate the trouble.

> <span id="page-33-3"></span>(1) *Voltage and resistance measurements.* These measurements will help locate the individual component at fault.

Use resistor and capacitor color codes [\(figs. 33](#page-48-0) and [34\)](#page-49-0) to find the value of the components. Use voltage and resistance diagrams [\(figs. 35-](#page-50-0)[37\)](#page-52-0) and charts in [paragraph 34](#page-43-0) to find normal readings and compare them with readings taken.

(2) *Troubleshooting chart.* The trouble symptoms listed in the chart [\(par. 32](#page-36-0)*c*) will

aid in isolating the trouble to a component part.

- (3) *Checking wave forms.* The procedure described in [paragraph 36](#page-45-0) will help to isolate the trouble to a component part.
- (4) *Intermittent troubles.* In all these tests, the possibility of intermittent troubles should not be overlooked. If present, this type of trouble often may be made to appear by



*Figure 23. Panel-chassis assembly, top view.*

tapping or jarring the equipment. Check the wiring and cables that connect the chassis to each other.

## <span id="page-35-0"></span>**30. Test Equipment Required**

The following chart lists the test equipment, the associated technical manuals, and the assigned common names.



# <span id="page-35-1"></span>**Section II. TROUBLESHOOTING RADAR TEST SET AN/UPM 60A**

### <span id="page-35-2"></span>*Caution:* **Do not attempt removal or replacement of parts before reading the instructions i[n paragraph 37.](#page-53-2)**

#### **31. Checking B- Circuits for Shorts**

*a. When to Check.* When any of the following conditions exist, check for short circuits and clear any troubles before applying power.

(1) When the radar test set has been received

- from a lower echelon and the nature of abnormal symptoms is not known.
- <span id="page-35-3"></span>(2) When abnormal symptoms reported from operational tests indicate possible power supply troubles.



*Figure 24. Panel-chassis assembly, bottom view.*
*b. Measurements.* Refer to the schematic diagram (fig. 62) for the B-distribution throughout the radar test set and the possible paths which could offer short circuits. By using the schematic diagram in conjunction with the voltage and resistance measurements in [figures 35](#page-50-0) through [37](#page-52-0) and [paragraph 34,](#page-43-0) the causes for troubles can be checked and isolated.

#### **32. Localizing Troubles**

*a. General.* In the troubleshooting chart (*c* below),

procedures are outlined for localizing troubles to a stage within the various sections of the radar test set. Parts locations are indicated i[n figures 23](#page-34-0) through [32](#page-47-0) Voltage and resistance measurements are shown in [Figures 35](#page-50-0) through [37 a](#page-52-0)nd [paragraph 34](#page-43-0)*b*. Wave forms are shown in [figures 57](#page-70-0) through [60.](#page-73-0) The peak-to-peak value of each waveform is determined by using the calibrated voltage scale of each waveform. Depending upon the nature of the operational symptoms, one or more of the



*Figure 25. Panel-chassis assembly, left-side view.*

<span id="page-36-0"></span>AGO 2704A

localizing procedures will be necessary. When trouble has been localized to a particular stage, use voltage and resistance measurement to isolate the trouble to a particular part.

*b. Use of Chart.* The troubleshooting chart is designed to supplement the equipment performance checklist in TM 11-6625-228-12. If operational checks result in a symptom that is listed in the chart, perform the correction given.

If no operational symptoms are known, begin with item 1 of the equipment performance checklist and proceed until a symptom of trouble appears.

*Caution:* **If operational symptoms are not known, or if they indicate the possibility of short circuits within the radar test set, make the short-circuit checks described in [paragraph 31](#page-35-0) before applying power to the unit.**



**TM 11-6625-228-35**



## <span id="page-39-0"></span>**33. Signal Substitution and Stage Gain, Pulse Amplifiers**

Pulse amplifiers V2 and V3 on main chassis assembly [\(fig. 29\)](#page-42-0) may be checked by substituting a signal and measuring the stage gain. Use Pulse Generator AN/UPM-15 as a signal source and use Oscilloscope AN USM-50 to measure stage output.

*a.* Apply a 1-millivolt signal from the pulse generator to the control grid (pin 1) of V2. With the oscilloscope, measure the signal at pin 5. The stage

should have a gain of about 27 decibels (db). Repeat this check for stage V3. The gain should be about 33 db. If the gain of any stage is too low, replace the tube.

*b.* To measure the overall gain of the pulse amplifiers, apply a 1-millivolt signal from the pulse generator to the control grid (pin 1) of V2 and measure the output, with the oscilloscope, at the plate (pin 5) of V3. The amplitude of the output wave form should be about 1 volt, indicating an overall gain in the amplifiers of about 60 db.



*Figure 26. Panel-chassis assembly, right-side view.*

<span id="page-39-1"></span>AGO 2704A



<span id="page-40-0"></span>*Figure 27. Rear of panel-chassis assembly, right oblique view.*



<span id="page-41-0"></span>*Figure 28. Front panel, rear view.*



<span id="page-42-0"></span>*Figure 29. Main chassis assembly, front panel removed.*



<span id="page-42-1"></span>*Figure 30. Modulator chassis, top view.*

180K<br>5K

180K 750K<br>5K

16.5K<br>INF

16.5K<br>**INF** 

350K<br>220K

Tube | Pin | Dc voltage to ground | Resistance to ground

3 2.6 47 4  $-90$  3M 5 220 340K<br>6 2.7 47 6 2.7 47 7 0 0 8 0 0 V6 | 1 | -85 | 3M [\(fig. 27\)](#page-40-0)  $\begin{array}{|c|c|c|c|}\n\hline\n2 & 220 & 30K \\
\hline\n3 & 2.7 & 47\n\end{array}$ 

3 2.7 47 4 -280 -240K  $\begin{array}{c|c|c|c|c|c} 5 & -37 & 350K \\ 6 & -200 & 15K \end{array}$ 6 -200 15K 7 0 0

V5 | 1 | -85 | 3M  $(fig. 27)$  2 220 340K

## <span id="page-43-0"></span>**34. Isolating Trouble Within Stage**

 $\overline{a}$ 

When trouble has been localized to a stage, either through operational checks or signal substitution [\(par. 33\),](#page-39-0) use the following techniques to isolate the defective part:

*a.* Test the tube involved, either in the tube tester or by substituting a similar type tube known to be operating normally.

*b.* Take voltage measurements at points related to the stage in question [\(figs. 35-](#page-50-0)[37\)](#page-52-0) and at the tube sockets listed below.

*c.* Notes 1 through 7 below indicate the normal setting of controls during voltage and resistance measurements.



For explanation of footnotes see [page 43.](#page-45-0)



For explanation of footnotes see [page 43.](#page-45-0)



<sup>a</sup> Voltages measurements taken between pins 2 and 7.

**b** Designates SYNC SELECTOR in EXT SINE EXT NEG position.

c Designates SYNC SELECTOR in EXT POS position.

<sup>d</sup> Designates SYNC SELECTOR in INT X 1 position.<br><sup>e</sup> Designates SYNC SELECTOR in INT X 10 position.

f Designates MODULATION SELECTOR in CW position.

<sup>g</sup> Designates MODULATION SELECTOR in PULSE position.

h Designates MODULATION SELECTOR in FM X 10 position.

i Designates all positions of the MODULATION SELECTOR switch.

j Designates DELAY MULTIPLIER in X 10 position.

*d.* If voltage readings are abnormal, take resistance readings to isolate open or short circuits. Refer also to the dc resistances of transformers and coils in [paragraph 35.](#page-45-1)

<span id="page-45-1"></span>*e.* Use the schematic diagram (fig. 62) to trace circuits and to locate the faulty component.

#### **35. Dc Resistances Transformers and Coils**

The dc resistances of the transformers and coils in the radar test set are listed below:





#### **NOTES**

**1. SYNC SELECTOR in EXT RF position.**

**2. RATE control in 150 position.**

**3. DELAY MULTIPLIER in X 1 position.**

**4. DELAY control in full CCW position.**

**5. PULSE WIDTH in .5 position.**

**6. MODULATION SELECTOR in FM X 1 position.**

**7. FUNCTION SELECTOR in RECV position.**

**8. For voltage and resistance measurements use 20,000 ohm per volt meter.**



#### **36. Checking Waveforms**

<span id="page-45-0"></span>Troubles that do not permit rapid localization to a stage through operational test can be localized by checking waveforms. [Figures 57](#page-70-0) through [60](#page-73-0) show the waveforms that should exist at the tube sockets. Using the oscilloscope, compare the waveforms at the various points indicated with those shown in the figures. If a difference is noted, make voltage and resistance measurements at that point to isolate the defective part.



<span id="page-46-0"></span>*Figure 31. Modulator chassis, top oblique view, cover open.*



<span id="page-47-0"></span>*Figure 32. Modulator chassis, top view, cover open.*

## RESISTOR COLOR CODE MARKING (MIL-STD RESISTORS)



## AXIAL-LEAD RESISTORS **RADIAL-LEAD RESISTORS** (INSULATED) (UNINSULATED)



#### RESISTOR COLOR CODE



\* FOR WIRE-WOUND-TYPE RESISTORS, BAND A SHALL BE DOUBLE-WIDTH. WHEN BODY COLOR IS THE SAME AS THE DOT (OR BAND) OR END COLOR, THE COLORS ARE DIFFERENTIATED BY SHADE, GLOSS, OR OTHER MEANS.<br>EXAMPLES (BAND MARKING): EXAMPLES (BAND MARKING): EXAMPLES (BODY MARKING): 10 OHMS ±20 PERCENT: BROWN BAND A; BLACK BAND B; 10 OHMS ±20 PERCENT BROWN BODY; BLACK END; BLACK DOT BLACK DOT<br>10 OR BAND BORN BAND BAND D. COLOR ON TOLERANCE END. BLACK BAND C; NO BAND D.<br>4.7 OHMS ±5 PERCENT: YELLOW BAND A; PURPLE BAND B; 3,000 OHMS ±10 PERCENT: ORANGE BODY, BLACK GOLD BAND C; GOLD BAND D. STD-R1 (SOLD BAND); SILVER END. STD-R1 (STD-R1)

3,000 OHMS ±10 PERCENT: ORANGE BODY, BLACK END; RED DOT OR BAND; SILVER END.

*Figure 33. MIL-STD resistor color-code markings.*

## CAPACITOR COLOR CODE MARKING (MIL-STD CAPACITORS)



## CAPACITOR COLOR CODE



1. LETTERS ARE IN TYPE DESIGNATIONS GIVEN IN MIL-C SPECIFICATIONS.

2. IN PERCENT, EXCEPT IN UUF FOR CC-TYPE CAPACITORS OF 10 UUF OR LESS. STD-C1 STD-C1

3. INTENDED FOR USE IN CIRCUITS NOT REQUIRING COMPENSATION.

# *Figure 34. MIL-STD capacitor color-code markings.*





TM6625-228-35-33

<span id="page-50-0"></span>*Figure 35. Resistor-capacitor mounting boards, TB1 and TB101, voltage and resistance diagram.*

AGO 2704A







*Figure 36. Resistor-capacitor mounting boards, TB 102 and TB3, voltage and resistance diagram.*







<span id="page-52-0"></span>*Figure 37. Resistor-capacitor mounting boards, TB103 and TB104, voltage and resistance diagram.*

#### **Section I. REPAIRS**

#### **37. General Parts Replacement Techniques**

Many of the parts of the radar test set can be reached and replaced easily without special procedures. The tube sockets, large capacitors, and inductors are mounted to the main chassis with hexagonal nuts and fillister or binding head screws. The following instructions apply specifically to the test set:

*a.* Variable attenuators AT2 and AT3, fixed attenuator AT1, frequency meter Z2, and thermistor mount Z1 are calibrated parts and should be replaced as complete assemblies if defective. Variable attenuator AT2 and frequency meter Z2 are replaced complete with their individually calibrated dials. These waveguide components are located on the rear of the front panel [\(fig. 28\)](#page-41-0).

*b.* To reach the tube sockets and terminal boards in the modulator chassis, unscrew the three cam lock studs and lift the hinged door [\(fig. 32\).](#page-47-0) If any of the switch wafers in the modulator chassis require replacement, carefully mark the wires with tags to avoid misconnection when the new switch is installed. Follow this practice whenever replacement requires the disconnection of several wires.

*c.* When replacing tubes, be sure that the power cable is not plugged into the POWER INPUT connector. This is important when removing the klystron.

<span id="page-53-0"></span>*Caution:* **A washer type RF ground (metex) is used in each RF choke joint. Be very careful during assembly and disassembly of RF components so as not to damage them.**

## **38. Removal and Replacement of Frequency Meter Z2**

[\(fig. 38\)](#page-54-0)

To remove the frequency meter-

*a.* Loosen the two No. 6-32 setscrews (1) on the small loaded gear.

*b.* Remove the eight No. 6-32 capscrews (2 and 5) lockwashers (3 and 4) that connect the frequency meter to the thermistor mount and fixed attenuator AT1.

*c.* Remove the three No. 8-32 binding head screws (6) and lockwashers (7) from the collar.

*d.* Loosen the No. 8-32 binding head screw  $(8)$  on the split collar.

*e.* Spread the split collar and remove the frequency meter. Retain the meter rings for replacement.

*f.* To replace the frequency meter, follow the removal procedure above in reversed order.

#### **39. Removal and Replacement of Waveguide Components**

The test set is a panel-frame-chassis assembly with the waveguide components mounted on the rear of the front panel [\(fig. 28\).](#page-41-0) To reach some of the waveguide components, separate the panel from the frame and chassis as follows:

*a.* Remove the pin from each of the four captive rods.

*b.* Remove the four captive rods.

*c.* Remove the four hexagonal nuts that secure the captive rod assemblies to the panel and frame.

*d.* Disconnect jack J8 and plugs P3, P7, P100, P102, P103, and P104.

*e.* Loosen the No. 8-32 setscrews on the seven knobs at the top of the panel and remove the knobs.

*f.* Remove the four No. 6-32 flathead screws that hold the modulator chassis to the frame.

*g.* Remove the four No. 10-32 binding head screws, lockwashers, and nuts that hold the panel to the frame (located in the corners of the front panel) and the three that hold the modulator chassis to the panel (located under the first, fourth, and seventh knob at the top of the panel).

*h.* Remove the modulator chassis.

*i.* Remove the No. 8-32 flathead screw, lockwasher, and nut that hold the fan baffle to the frame.



2 Capscrew 6-32 3 Lockwasher No. 6 4 Lockwasher No. 6 6 Binding head screw 8-32 7 Lockwasher No. 8 8 Binding head screw 8-32

10 Collar assembly 11 Capscrew 6-32 12 Lockwasher No. 6 14 Capscrew 6-32 15 Capscrew 6-32 16 Lockwasher No. 6

<span id="page-54-0"></span>

*f.* Remove the four No. 10-24 binding head screws and lockwashers that are behind the handles on the front panel.

*k.* To disconnect the front panel assembly, first pull out the left side slightly and then bend the fan baffle inwardly.

*l.* To replace the panel to the frame and chassis, reverse the removal procedure.

<span id="page-55-0"></span>*m.* The removal of the individual waveguide components is described in [paragraphs 40](#page-55-0) through [45.](#page-57-1)

#### **40. Removal, Replacement, and Calibration of Rotary Attenuator AT2**

- *a.* To remove the rotary attenuator-
	- (1) Remove the front panel from the test set.
	- (2) Unscrew the two screws that secure the line filter to the rear of the front panel and remove the line filter.
	- (3) Unscrew the eight allen-head screws that secure the U-bend to the attenuator casting and carefully remove the U-bend.
	- (4) Remove the upper and lower bearings from the ends of the upper and lower rotary attenuator, respectively.
	- (5) Loosen the two allen-head setscrews on the worm gear and loosen the two allenhead setscrews on each of the rotary attenuator gears.
	- (6) Push the worm gear assembly down and tighten the allen-head lockscrew to hold the worm gear assembly away from the worm gear.
	- (7) Withdraw the two rotary attenuators approximately 1 inch and remove the upper and lower attenuator gears.
	- (8) With the lower rotary attenuator withdrawn about 2 inches, slide the worm gear to the right off the rotary attenuator, and remove it.
	- (9) Remove the upper and lower square flange adapter bearings.
	- (10) Withdraw completely the upper and lower rotary attenuators.
- *b.* To replace the rotary attenuators-
	- (1) Insert the upper square flange adapter bearing.
	- (2) Insert the upper rotary attenuator through the attenuator casting (thick rim first),

through the upper attenuator gear, and work into the upper square flange adapter bearing.

- (3) Insert the lower square flange adapter bearing.
- (4) Insert the lower rotary attenuator through the attenuator casting (thin rim first), through the worm gear, through the lower attenuator gear, and work it into the lower square flange adapter bearing.
- (5) Tighten the allen-head setscrews on the upper and lower attenuator gears and worm gear.
- (6) Loosen the allen-head lockscrew on the worm gear assembly and engage the worm gear with the worm gear assembly.
- (7) Calibrate the rotary attenuator, starting with *c* below.
- *c.* To calibrate the rotary attenuator-
	- (1) Remove the front panel from the test set.
	- (2) Unscrew the two screws that secure the line filter to the rear of the front panel and remove the line filter.
	- (3) Unscrew the eight allen-head screws that secure the U-bend to the attenuator casting and carefully remove the U-bend.
	- (4) Remove the upper and lower bearings from the ends of the upper and lower rotary attenuators, respectively.
	- (5) Unscrew the four screws that secure the RF INPUT waveguide to the rear of the front panel.
	- (6) Unscrew the four allen-head screws that secure the RF INPUT waveguide to the lower square flange adapter.
	- (7) Unscrew the four allen-head screws that secure the U-waveguide to the crystal mount assembly and remove the RF INPUT and U-waveguide.
	- (8) Unscrew the four allen-head screws that secure the half-U-waveguide to the upper square flange adapter.
	- (9) Unscrew the four allen-head screws that secure the half-U-waveguide to the power set attenuator assembly and remove the half-U-waveguide.
	- (10) Loosen the two allen-head setscrews on the worm gear.
	- (11) Look into the open end of the lower

rotary attenuator and aline it so that the resistance card and the bracket to which it is glued coincide exactly with the resistance card and bracket in the lower square flange adapter.

- (12) Set the attenuator dial to a +6.0 (RED) reading and tighten the two allen-head setscrews on the worm ear.
- (13) Loosen the two allen-head setscrews on the worm gear assembly hub and turn hub clockwise (when viewed from the rear of the front panel) until the hub turns no further.
- (14) Recheck the attenuator dial for a +6.0 (RED) reading and tighten the two allenhead setscrews on the worm gear assembly hub.
- (15) Loosen one of the allen-head screws on the upper attenuator gear.
- (16) Turn the attenuator knob until the second allen-head setscrew can be reached. Loosen the second setscrew.
- (17) Set attenuator dial to +6.0 (RED).
- (18) Look into the open end of the upper rotary attenuator and rotate it manually until the upper rotary attenuator resistance card and bracket exactly coincide with the resistance card and bracket of the upper square flange adapter.
- (19) Slide the upper attenuator gear on the rim of the upper rotary attenuator and turn the upper attenuator gear until it is in exactly the same position as the attenuator gear on the lower rotary attenuator.
- (20) Slide the upper attenuator gear back on the rim of the upper rotary attenuator and tighten the allen-head setscrew.
- (21) Rotate the attenuator knob until the second allen-head setscrew can be reached and tighten the second allenhead setscrew.

## <span id="page-56-0"></span>**41. Removal and Replacement of POWER SET Attenuator AT3**

[\(fig. 38\)](#page-54-0)

To remove the power set attenuator-

*a.* Loosen the two No. 8-32 setscrews on the POWER SET switch knob and the two No. 8-32 setscrews on the FUNCTION SELECTOR switch knob. Remove the knobs.

*b.* Loosen the two No. 4-40 setscrews (9) of the collar assembly (10) on the FUNCTION SELECTOR switch shaft.

*c.* Remove the 16 No. 6-32 capscrews (5, 11, 14, and 15) and lockwashers (4, 12, 13, and 16) that connect the power set attenuator to the waveguide system and frequency meter. Remove fixed attenuator AT1.

*d.* Remove the No. 6-32 capscrew, lockwasher, flat washer, and cable clamp that hold the cable to the power set attenuator.

*e.* Remove the two No. 4-40 capscrews, lockwashers, and flat washers that hold the crystal bracket to the power set attenuator [\(fig. 25\)](#page-36-0).

*f.* Remove the three No. 10-32 capscrews and lockwashers (located between the FUNCTION SELECTOR switch and POWER SET switch) that hold the power set attenuator and microswitch bracket to the casting. Leave the bracket hanging and slide out the power set attenuator from the casting. Remove the collar assembly from the shaft and retain it for replacement.

*g.* To replace the power set attenuator, follow the removal procedure above in reversed order.

## **42. Removal and Replacement of Fixed Attenuator AT1** [\(fig. 38\)](#page-54-0)

*Note***. This component can be removed without disassembling the panel-frame-chassis assembly.**

To remove the fixed attenuator-

*a.* Remove the eight No. 6-32 capscrews (5 and 14) and lockwashers (4 and 13) that connect the fixed attenuator to the power set attenuator and frequency meter.

*b.* Remove the fixed attenuator from the side of the unit Retain the frequency meter rings for replacement.

<span id="page-56-1"></span>*c.* To replace the fixed attenuator, follow removal procedure above in reversed order.

## **43. Removal and Replacement of Thermistor Mount Assembly Z1** [\(fig. 38\)](#page-54-0)

## *Note.* **This component can be removed without disassembling the panel-frame-chassis assembly.**

To remove the thermistor mount assembly-

*a.* Unsolder and tag the four wires to the thermistor mount terminal board [\(fig. 26\)](#page-39-1).

*b.* Remove the four No. 6-32 capscrews (2) and lockwashers (3) that connect the thermistor mount assembly to the frequency meter. (To remove the capscrews tilt them.).

*c.* Remove the two No. 8-32 capscrews and No. 8 lockwashers that hold the thermistor mounting bracket in place. To remove the thermistor mount assembly, clear the waveguide bracket and slide the component down and out from the side of the unit.

<span id="page-57-0"></span>*d.* To replace the thermistor mount assembly, follow the removal procedure above in reversed order.

## **44. Removal of Klystron**

[\(fig. 39\)](#page-58-0)

#### *Note.* **This component can be removed without disassembling the panel-frame-chassis assembly.**

To remove the klystron-

*a.* Disconnect klystron jack J9 [\(fig. 28\)](#page-41-0).

*b.* Loosen the two No. 8-32 setsrews (1) on the right angle drive gear. Slide out the short shaft (2) that connect the klystron tube. Retain shaft for replacement.

*c.* Remove the four No. 6-32 capscrews (3) and lockwashers (4) that connect the klystron housing to the waveguide. Remove the klystron housing by lifting it and clearing the shaft from the right angle drive.

*d.* Leave the meter ring in the waveguide.

<span id="page-57-1"></span>*e.* Remove the tube from the housing by removing the four No. 4-40 pan head screws (5) and lockwashers (6).

*f.* Leave the meter ring in the housing.

#### **45. Replacement of Klystron**

[\(fig. 39\)](#page-58-0)

To replace klystron-

*a.* Set the klystron shaft at seven-sixteenths of an inch.

*b.* Reverse the procedure in [paragraph 44](#page-57-0)*c* and *e*.

*c.* Turn right angle drive shaft completely clockwise and replace short shaft (2) so that it is engaged in the slot. Tighten the two No. 8-32 setscrews (1) on the right angle drive gear.

*Caution:* **Do not screw shaft beyond the point at which resistance is encountered. Failure to observe this precaution may result in destruction of the klystron.**

## **46. Checking Oscillating Range of New Klystron**

One of two methods (*a* and *b* below) may be used to determine if the new klystron covers the frequency range of the test set.

- *a. Using Oscilloscope and Crystal Detector.*
	- (1) Using Oscilloscope AN/USM-50 and the power mount, connect the equipment as shown in [figure 40.](#page-59-1) Set the controls as follows:



- (2) Allow the test set to warm up for 1 hour. When the set is temperature stabilized, proceed as follows:
	- (*a*) Use the oscilloscope controls to present the klystron mode pattern completely on the screen.
	- (*b*) Vary the REFLECTOR control until a maximum signal appears on the screen of the oscilloscope.
	- (*c*) Check the frequency at the low end of the dial by rotating the WAVE-METER TUNING control until a dip appears directly in the center of the mode curve. Read the WAVE-METER FREQUENCY dial. If the frequency is higher than 15,750 megacycles (mc), loosen the set screws on the drive hub. While maintaining pressure against the stop washers, rotate the OSCILLATOR TUNING control counterclockwise. If no frequency dip is obtainable, reject the tube for use in the test set. If a frequency indication is obtained, tighten the setscrews. If the frequency is 15,750 mc or lower, proceed with the operations in (*d*) through (*f*) below.
	- (*d*) Turn the OSCILLATOR TUNING control completely clockwise.
- (*e*) Repeat the procedure in (b) above.
- (*f*) Rotate the WAVEMETER TUNING control until a dip appears in the center of the hump. If the frequency dial reads over 16,250 mc, the tube can be used in the radar test set. If the frequency is not over 16,250 mc, reject the tube.
- *b. Using Test Set Panel Meter.* (1) Set the controls as follows:





<span id="page-58-0"></span>*Figure 39. RF waveguide assembly, right side view.*

1 Setscrew 8-32

(2) Allow the test set to warm up for 1 hour. When the test is temperature stabilized, perform the operations given in *a* above; observe the deflection of the meter needle instead of the oscilloscope. A dip in the meter is an indication that the wavemeter is tuned to resonance.

*Note.* **The REFLECTOR control is adjusted for maximum panel meter reading.**



<span id="page-59-1"></span>*Figure 40. Test setup for checking new klystron and pulse width.*

## **Section II. ADJUSTMENTS**

## **47. General**

All controls to be used for adjustments are screwdriver adjusted potentiometers on the main and modulator chassis and can be reached when the test set is removed from the carrying case. The locations of these controls are shown in [figures 23](#page-34-0) through [32.](#page-47-0) Test equipment required is listed in [paragraph 48.](#page-59-2) To test set properly, follow the procedures, in the order given, in [paragraphs 49](#page-59-0) throug[h 57.](#page-62-0)

<span id="page-59-2"></span>*Note.* **Before starting the adjustments, allow the test set to warm up for at least 1 hour (with the POWER switch up).**

#### **48. Test Equipment Required for Adjustment**

The following chart lists the test equipment, the associated technical manuals, and the assigned common names.



<span id="page-59-0"></span>\*The PRD type 616 crystal detector is part of Standing Wave Indicator TM-97/USM-37.

#### **49. Adjustment of Regulated B- Voltages**

The regulated B-voltages (-300 and 200 volts) provide a part of the stability of the radar test set; therefore, it is important that these voltages be set correctly as instructed below before further adjustments are made.

*a.* Clip the positive multimeter prod to the chassis and the negative prod to the high side of capacitor C14.

*b.* Adjust -300V ADJ R48 [\(fig. 23\)](#page-34-0) for a reading of 300 volt on the meter.

*c.* Set the POWER switch to the HEATER position.

*d.* Clip the positive multimeter prod to pin 6 of V6B and the negative prod to the low side of R66.

*e.* Set the POWER switch to the POWER position. After temperature stabilization, adjust 200V ADJ R59

[\(fig. 23\)](#page-34-0) for a 200-volt reading on the meter. This reading should remain constant with variations of REFLECTOR control R64.

#### **50. Adjustment of V109 Bias**

With insufficient bias, V109 will free run. The proper bias is obtained by adjusting the V109 BIAS ADJ R188.

*a.* Remove V109.

*b.* Connect the multimeter between the grid and the cathode of V109.

*c.* Adjust R188 so that the bias voltage is -15 volts.

*d.* Replace V109.

## **51. Adjustment of AM ADJ Control**

For proper operation of the equipment when the output is pulse modulated, adjust the AM adj (R209) as follows:

*a. Test Setup.* The power mount and the oscilloscope are required for this test. Connect the equipment as shown in [figure 41.](#page-60-0)

*b. Preliminary Procedure.* Obtain a 1-milliwatt reference level at 16,000 mc as described in TM 11-6625-228-12.

*c. Test Control Settings.*



- *d. Test Procedure.*
	- (1) Set the controls on the oscilloscope so that 1 complete cycle can be observed on the screen.
	- (2) Adjust R209 for optimum rise and decay times, while keeping the amplitude between 25 and 40 volts.



<span id="page-60-0"></span>*Figure 41. Test setup for AM adjustment.*

#### **52. Pulse Width Adjustment**

The pulse width of the pulsed RF output can be adjusted by using the front panel PULSE WIDTH control R194 and may be varied continuously up to 2 microseconds. To insure that this control is calibrated properly, the maximum width of the pulse is adjusted with WIDTH ADJ R198 [\(fig. 30\)](#page-42-1) as follows:

*a. Test Setup.* The power mount and the oscilloscope are required for this test. Connect the equipment as shown i[n figure 40.](#page-59-1)

*b. Test Set Control Settings.*



*c. Procedure.*

- (1) Measure the pulse width on the oscilloscope screen at the half-power points.
- (2) Adjust this width to equal 2 microseconds with WIDTH ADJ R198 [\(fig. 30\)](#page-42-1).

## **53. Repetition Rate Adjustment**

When the test set is internally triggered, the pulse or FM repetition rates may be continuously varied from 100 to 10,000 cycles per second by means of the two internal positions of the SYNC SELECTOR switch and the setting of the RATE control. For proper calibration of the RATE control for either position of the SYNC SELECTOR switch, the pulse repetition rate is adjusted at both ends of the range with internal screwdriver controls 100 PPS ADJ R166 and 10,000 PPS ADJ R169 [\(fig. 30\)](#page-42-1) as described below.

*a. Test Setup.* The frequency meter is required for this test. Connect the equipment as shown in [figure 42.](#page-61-0)

- *b. Test Procedure.*
	- (1) Set the SYNC SELECTOR switch to INT X 1.
	- (2) Set the RATE control to 100.
- (3) Adjust internal screwdriver control 100 PPS ADJ R166 [\(fig. 30\)](#page-42-1) until the frequency meter reads 100 pps.
- (4) Repeat the procedures in (1) through (3) above for the maximum end of the repetition rate range, but set the SYNC SELECTOR switch to INT X 10 and the RATE control to 1000 maximum, and adjust internal screwdriver control 10,000 PPS ADJ R169 until the frequency meter reads 10,000 pps.

## **54. Delay Adjustment**

When the test set is internally triggered, the output pulse or the initiation of the FM sweep may follow the internal trigger by an interval continuously variable from 1 microsecond to 1,000 microseconds or up to 90 percent of the interval between pulses, whichever is less. This interval is controlled by the front panel DELAY and DELAY MULTIPLIER controls. For proper calibration of the DELAY control for either position of the DELAY MULTIPLIER switch, two internal potentiometer controls, MAX DELAY ADJ R131 and DELAY MULT ADJ R142, are provided. Adjust these controls as follows:

*a. Test Set Control Settings*.





TM6625-228-35-40

<span id="page-61-0"></span>

AGO 2704A

- *b. Test Setup.* An oscilloscope is required for this adjustment. Connect the equipment as shown in [figure 43.](#page-61-1)
- *c. Test Procedure.*
	- (1) Observe the position of the pulse on the oscilloscope trace. Since the sweep is initiated by the undelayed sync pulse, the position of the delayed sync pulse above the trace is an indication of the delay interval between these pulses.
	- (2) Adjust the interval between the undelayed sync pulse and the delayed sync pulse when that interval, as established by the DELAY MULTIPLIER and DELAY controls, is 100 microseconds and 1,000 microseconds. Use the appropriate internal potentiometer control for each setting; that is, MAX DELAY ADJ R131 for the 100 microseconds setting and DELAY MULT ADJ R142, for the 1,000 microsecond setting. In each case, the sweep time control of the oscilloscope should be set properly.

## **55. ZERO SET Adjustment**

<span id="page-61-2"></span>Set the FUNCTION SELECTOR switch in the TRANS position. Adjust COARSE ZERO SET ADJ R11 [\(fig. 23\)](#page-34-0) so that a zero reading can be obtained by rotating the front pan ZERO SET control. During this adjustment, no RF energy should be fed into the test set.

## **56. RECV SENS ADJ Control Adjustment**

When the test set is operated in the RECV position, RECV SENS ADJ R3 is adjusted so that a 1-milliwatt RF output level is obtained at 16,000 mc.



TM6625-228-35-41

<span id="page-61-1"></span>*Figure 43. Test setup for delay adjustment.*

*a.* Connect the test set as shown in [figure 44.](#page-62-2)

*b.* Obtain a 1-milliwatt reference level as described in TM 11-6625-228-12.

*c.* Adjust the RECV SENS ADJ R3 until 1 milliwatt is indicated on the power meter.

<span id="page-62-0"></span>*d.* Repeat *b* above for frequencies of 15,750 and 16,250 mc and record the error*.*

## **57. TRANS SENS ADJ. Control Adjustment**

*a.* Connect the test set as shown in [figure 45.](#page-62-1)

*b.* Obtain a 1-milliwatt reference level at 16,000 mc as described in TM 11-6625-228-12.

*c.* With zero power from the signal generator, turn the FUNCTION SELECTOR switch to TRANS position and adjust the zero set for a 0-meter reading.

*d.* Adjust the output of the signal generator for a frequency of 16,000 mc and for a .1-milliwatt indication on the power meter.



<span id="page-62-2"></span>*Figure 44. Test setup for adjustment of RECV SENS ADJ control.*

*e.* Turn the ATTENUATOR control until the DBM POWER scale indicates +6 on the red scale.

*f.* Adjust R4 until the test set meter indicates 1 milliwatt.

*g.* Adjust the output of the signal generator for a 1 milliwatt indication on the power meter.

*h.* Record the error as read on the red scale. The maximum error is 10 dbm.

*i.* Repeat the above procedures at the +10 dbm level.

*j.* Repeat the above procedures for the frequencies of 15,800 mc and 16,200 mc.



<span id="page-62-1"></span>*Figure 45. Test setup for adjustment of TRANS SENS ADJ control.*

#### **58. Purpose of Final Testing**

The tests outlined in this section are designed to measure the performance capability of a repaired equipment. Equipment that meets the minimum standards stated in the tests will furnish satisfactory operation, equivalent to that of new equipment.

## **59. Test Equipment Required for Final Testing**

The following chart lists test equipment required for final testing, the associated technical manuals, and the assigned common names.



\* PRD type 616 crystal detector is part of IM-97/USM-37.

#### **60. Operational Test**

*a.* Operate the test set as described in TM 11-6625-228-12.

*b.* Using the oscilloscope and the crystal detector (PRD type 616), connect the equipment as shown in [figure 46.](#page-64-1)

*c.* Obtain a 1-milliwatt reference level at 15,750 mc as described in TM 11-6625-228-12.

*d.* Set the front panel controls as follows:



*Note***. Observe the frequency range of the test set on the WAVEMETER FREQUENCY dial and the**

## **oscilloscope presentation to insure that the unit is operating properly.**

*e.* Tune the wavemeter until a dip is seen in the center of the pulse. This indicates that the klystron is oscillating at 15,750 mc.

*f.* Simultaneously turn the OSCILLATOR TUNING control slowly clockwise and the REFLECTOR control to maximize the signal; then tune the wavemeter for a dip in the center of the pulse.

*g.* Repeat the procedure above until a frequency of 16,250 mc is reached.

#### **61. Power Output Test**

*a.* Operate the test set as described in TM 11-6625-228-12.

*b.* Connect the equipment as shown in [figure 47.](#page-64-0)

*c.* Disconnect C124 from the plate (pin 6) of V108A and feed the output of the square wave generator through C124.

*d.* Set the square wave generator for a 1,000-cps output.

*e.* Obtain a 1-milliwatt level at 15,750 mc as described in TM 11-6625-228-12.

*f.* Set the MODULATION SELECTOR switch to FM X 1 or FM X 10.

*g.* Set the rotary attenuator at 50 db.

*h.* Tune the receiver to the RF output of the test set.

*i.* Adjust the standing wave indicator for a convenient setting on the standing wave indicator.

*j.* Turn the ATTENUATOR control until POWER DBM scale indicates -10.

*k.* Adjust the rotary attenuator until the indication on the standing wave indicator is restored to its reference value (*i* above). Record the error on the rotary attenuator.

*l.* Repeat the procedures above in 10-dbm steps until -90 dbm is obtained.

*m.* Repeat the procedures above at frequencies of 16,000 mc and 16,250 mc.

## *Note***. Algebraically add the 0-dbm error [\(par. 56\)](#page-61-2) to this data at 15,750 mc and 16,250 mc.**

## **62. Cw Test**

Check the cw signal for the presence of incidental FM and AM. The maximum allowable incidental FM is .3 mc and the maximum allowable AM incidental is .5 db.

*a.* To check the incidental FM-

- (1) Operate the test set as described in TM 11-6625-228-12.
- (2) Connect the equipment as shown in [figure 48.](#page-64-2)
- (3) Obtain a 1-milliwatt reference level at 15,750 mc as described in TM 11-6625-228-12.
- (4) Read the frequency deviation on the spectrum analyzer.



<span id="page-64-1"></span>*Figure 46. Test setup for operational test.*

(5) Repeat the test at 16,250 mc.

- *b.* To check the incidental AM-
	- (1) Connect the equipment as shown in [figure 49.](#page-65-0)
	- (2) Repeat the procedure *a*(3) above.

*Note***. The fractional amplitude modulation** *(A)* **is equal to the maximum amplitude** *(B)* **seen on the oscilloscope minus the cw level amplitude** *(C)* **divided by the** *CW* **level amplitude** *(C).*

*B ¾ C* Therefore  $A =$  and the incidental *C* AM in db is equal to 20  $log_{10}A$ .

- (3) Obtain the above data and calculate the incidental AM at 15,750 mc.
- (4) Repeat this test at 16,250 mc.



<span id="page-64-0"></span>



<span id="page-64-2"></span>*Figure 48. Test setup for measuring incidental FM and FM frequency deviation.*



<span id="page-65-0"></span>*Figure 49. Test setup for measuring incidental AM.*

# **63. Pulse Modulation Test**

Check the repetition rate range, pulse width, and pulse delay as described below. The unit specification requires that the repetition rate ranges are from 100 to 1,000 cps and 1,000 to 10,000 cps. The pulse width range is from .2 to 2 microseconds and the pulse delay is greater than 90 percent of the time interval between pulses.

*a.* To check the repetition rate range--

- (1) Operate the test set as described in TM 11-6625-228-12.
- (2) Connect the equipment as shown in [figure 50.](#page-65-1)
- (3) Obtain a 1-milliwatt reference level at 16,000 mc as described in TM 11-6625-228-12.
- (4) Set the front panel controls as follows:



- (5) Read the frequency meter.
- (6) Set the RATE control to 1,000.
- (7) Repeat (5) above.
- (8) Set the SYNC SELECTOR switch to INT  $X$  10.
- (9) Repeat (5) above.
- (10) Set the RATE control to 100.
- (11) Repeat (5) above.
- *b.* To check pulse width-
	- (1) Connect the equipment as shown in [figure 51.](#page-66-0)
	- (2) Set the front panel as follows:



## *Note***. The reading of the pulse width is taken at the 50 percent amplitude points.**

- (3) Check the pulse width indicated on the oscilloscope.
- (4) Reset the PULSE WIDTH control to 2.
- (5) Repeat *b* (3) above.
- *c.* To check the pulse delay-
	- (1) Connect the equipment as shown in [figure 51.](#page-66-0)
	- (2) Reference the undelayed sync output to the beginning of the oscilloscope sweep.
	- (3) Obtain three pulses on the screen at 10,000 cps and measure the maximum delay obtainable.
	- (4) Set the front panel controls as follows:



(5) The delay as read on the screen should be at least 1,000 microseconds.

## **64. FM Tests**

Check the FM frequency deviation and FM delay as described below.

- *a.* To check the FM frequency deviation-
	- (1) Operate the test set as described in TM 11-6625-228-12.



<span id="page-65-1"></span>*Figure 50. Test setup for checking the pulse repetition rate range.*



<span id="page-66-0"></span>*Figure 51. Test setup for checking the pulse width and pulse delay.*

- (2) Connect the equipment as shown in [figure 48.](#page-64-2)
- (3) Set the front panel controls as follows:



- (4) Rotate the FM AMPLITUDE control until a minimum deviation of 12.5 mc from the center frequency is noted on the spectrum analyzer.
- (5) Repeat (4) above with the MODULATION SELECTOR switch set to FM X 10 and the SYNC SELECTOR switch set to INT X 10.
- *b.* To check the FM delay-
	- (1) Connect the equipment as shown in [figure 52.](#page-66-1)

*Note***. The test set should be continuously in phase, with respect to the trigger pulse, up to 1,000 microseconds or 90 percent of the time interval between trigger pulses, whichever is less.**

- (2) Obtain a 1-milliwatt reference level at 16,000 mc as described in TM 11-6625-228-12.
- (3) Set the front panel controls as follows:



## *Note.* **Reference the undelayed pulse to the beginning of the oscilloscope.**

- (4) Rotate the DELAY control from minimum to maximum delay. Check to see that the delay indicated on the oscilloscope is the same as that indicated by the DELAY control.
- (5) Reset the DELAY MULTIPLIER control to X10 and the DELAY control to 100. Check the oscilloscope for a 1,000 microsecond delay.



<span id="page-66-1"></span>*Figure 52. Test setup checking FM delay and synchronization.*

## **65. Synchronization**

Check the self-synchronization and the external synchronization and pulsed RF output signals as described below.

- *a.* To check the self-synchronization-
	- (1) Operate the test set as described in TM 11-6625-228-12.
	- (2) Connect the equipment as shown in [figure](#page-66-1) [52.](#page-66-1)
	- (3) Obtain a 1-milliwatt reference level at 16,000 mc as described in TM 11-6625-228-12.

(4) Set the front panel controls as follows:



- (5) Vary the RATE control over its entire range. Repeat this procedure with the SYNC SELECTOR switch set to INT X 10. While performing these operations, measure and check the pulse repetition rates.
- *b.* To check the external synchronization-
	- (1) Connect the equipment as shown in [figure 53.](#page-67-0)
	- (2) Repeat *a*(3) above.
	- (3) Set the front panel controls as described in *a*(4); exclude the SYNC SELECTOR switch.
	- (4) Set the SYNC SELECTOR switch to EXT POS.

*Note.* **The amplitude of the positive and negative pulses is 15 volts and the pulse width is 1 microsecond. The amplitude of the sine wave is 15 volts root mean square (rms).**

- (5) Feed an external positive pulse into the INPUT SYNC receptacle.
- (6) Check for the presence of a detected pulse as the input sync frequency is varied between 100 and 10,000 pps.
- (7) Set the SYNC SELECTOR switch to EXT SINE EXT NEG.
- (8) Feed an external negative pulse into the INPUT SYNC receptacle.
- (9) Repeat the procedure in *b*(6) above.
- (10) Feed an external sine wave into the INPUT SYNC receptacle.
- (11) Repeat the procedure in *b*(6) above.
- *c.* To check the pulsed RF output-
	- (1) Connect the equipment as shown in [figure 54.](#page-68-0)

## *Note.* **Use microwave signal generator Polarad model PMK.**

- (2) Set the front panel controls as described in *a*(4); exclude the SYNC SELECTOR switch.
- (3) Set the SYNC SELECTOR switch to EXT RF.
- (4) Adjust the signal generator so that the output pulse is at a 10-dbm level and is 2 microseconds wide.
- (5) Vary the RF input modulation frequency from 100 to 10,000 cps and observe the RF output frequency.

## **66. Trigger and Output Pulse Data**

*a*. Obtain the output trigger and pulse data by using the specified loads (5,000 ohms, 5,000 ohms in parallel with 1,500 micromicrofarads (μμf), 100,000 ohms and 100,000 ohms in parallel with 1,500 μμf) across the RF output connector. The equipment should meet the following requirements:

- (1) Amplitude between 20 and 50 volts positive polarity.
- (2) Pulse width between .5 and 1 microseconds (μsecs) at 50 percent amplitude points.
- (3) Rise time less than .5 μsecs as measured between 10 and 90 percent amplitude points.
- (4) Overshoot or ringing less than 5 percent.



<span id="page-67-0"></span>*Figure 53. Test setup for checking eternal synchronization.*

- (5) Decay time less than 3 μsecs as measured between 10 and 90 percent amplitude points.
- (6) Leading edge of trigger pulse should occur within -1 to +.25 μsecs of the leading edge of the RF output pulse as measured from 50 percent amplitude points.
- *b.* To check the trigger data-
	- (1) Place the test set in operation as described in TM 11-6625-228-12.
	- (2) Connect the equipment as shown in [figure 55.](#page-68-1)
	- (3) Obtain a 1-milliwatt reference level at 16,000 mc as described in TM 11-6625-228-12.
	- (4) Set the front panel controls as follows:



- (5) With the UNDELAYED OUTPUT SYNC connected to the oscilloscope, note the following characteristics: amplitude, polarity, pulse width, rise time, overshoot or ringing, and decay time.
- (6) Disconnect the UNDELAYED OUTPUT SYNC and connect the DELAYED OUTPUT SYNC to the oscilloscope. Repeat the measurement of the characteristics noted (*a*(5)).



<span id="page-68-0"></span>*Figure 54. Test setup for checking pulsed RF output.*

- *c.* To check the output pulse data-
	- (1) Connect the equipment as shown in [figure 46.](#page-64-1)
		- (2) Reference the 50 percent amplitude point of the delayed output pulse in the center of the oscilloscope sweep.
		- (3) Check the delay (+ or -) of the RF output pulses; use the leading edge (50 percent) of the delayed output

## **67. Frequency Measurement Tests**

*a.* Operate the test set as described in TM 11-6625-228-12.

*b.* Connect the equipment as shown in [figure 56.](#page-69-0)

*c.* Obtain a 1-milliwatt reference level at 15,750 mc as described in TM 11-6625-228-12.

## *Note.* **The second harmonic frequency is recorded when the two frequency marks are superimposed.**

*d*. Check and record the frequency which should be within the tolerances (technical characteristics) listed in TM 11-6625-228-12.

*e.* Repeat the above procedure from 15,750 mc to 16,250 mc 20-mc intervals.

## **68. RF leakage Test**

*a.* Operate the test set as described in TM 11-6625-228-12.

*b.* Obtain a 1-milliwatt reference level at 15,750 mc described in TM 11-6625-228-12.

*c.* Rotate the ATTENUATOR control until the POWER DBM scale reads -65.

*d.* Connect the RF output of the test set to the spectrum analyzer.



<span id="page-68-1"></span>*Figure 55. Test setup for checking trigger data.*

*Note.* **Use Waveguide Assembly CG-539/U to connect the RF output of the test set to the spectrum analyzer.**

*e.* Tune the spectrum analyzer to the input frequency signal; adjust and note the amplitude of the displayed signal.

*f.* Disconnect the setup indicated in *d* above and connect the termination waveguide to the RF OUTPUT jack.

*g.* Connect Waveguide Horn AT-531/UPM and Waveguide Assembly CG-539/U to the spectrum analyzer.

*h.* Move Waveguide Horn AT-531/UPM around the surfaces of the termination waveguide. All of the signals observed on the spectrum analyzer should be less than the amplitude observed as noted in *d* above.

*i.* Repeat the above procedure for 16,000 mc and 16,250 mc.



<span id="page-69-0"></span>*Figure 56. Test setup for checking frequency measurements.*



<span id="page-70-0"></span>*Figure 57. Waveform chart, modulator chassis, V101 through V103.*



*Figure 58. Waveform chart, modulator chassis, V104 through V106.*

AGO 2704A


*Figure 59. Waveform chart, modulator chassis, V107 through V110.*



*Figure 60. Waveform chart, modulator chassis, V111 and V112.*



*Figure 61. Rotary attenuator AT2, vane positions.*



*Figure 62. Radar Test Set AN/UPM-60A, schematic diagram.*

### **APPENDIX**

# **REFERENCES**



# **INDEX**















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*NG:* State AG (3); same as Active Army except allowance is one copy to each unit. *USAR:* None.

For explanation of abbreviations used, see AR 320-50.

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